Week	Dates	Lecture (Tentative)	Reading (Razavi)	Reading (GLHM)	Homework and Lab
1	08/28 08/30	• Administrative information • Intro/Overview: What is 140 all about? • Op-amps circuits in lab 1	Ch-1 Review Ch-§2.1-2.3	Page xiv symbol conventions 1.5, 1.6 MOS large & small signal models skim chapter 3	HW 1 Lab 1
2	09/04 09/06	• Taylor, Heaviside, and Bode • Diode, BJT, and MOS physics • MOS small signal model(s) and body effect	Ch-§2.4-2.6 (Skim 2.5 & 2.6)	Ch-§1.2	HW 2
3	09/11 09/13	• Common source single pole amplifiers • Frequency and step response	Ch-§3.1-3.4 (esp. figures 3.5, 3.6, 3.18-3.20) Ch-§6.2 through eqn 6.22	Ch-§7.1, 7.2.1 up through eqn.7.27 Ch-§3.1, 3.2, 3.3.2	HW 3 Lab 2
4	09/18 09/20	• Common source: input pole, input capacitance • Active load		3.3.5 (eqns. 3.55 and 66), 3.4.2.2 (eqns 3.126, 127, 128) Figure 4.17	HW 4 Lab 3 (part 1)
5	09/25 09/27	• Common gate: Review • Midterm 1: one sheet (two sides) of 8.5"x11" paper			
6	10/02 10/04	• Current mirrors, differential pair, differential amplifier	Ch-§5.1 (esp. figures §5.5, 5.7, 5.10 and 5.11) Ch-§4.1,4.2 through Figure-§4.14	Ch-§3.5.{3-5} MOS diff pair (eqn. 161, 171-174) (eqn. 188-191, 199-201) (Fig 3.51) Ch-§4.2.2.2 MOS current mirror (eqn. 17-20) 4.3.1, 4.3.5.2 Active loads (eqns 143, 149) Ch-§4.1,4.2 through Figure-§4.14	HW 5
7	10/09 10/11	• 2 stage op amp frequency response feedback, stability compensation	Ch-§6.2 Ch-§10.1-10.6	Ch-§6 read 6.1.1, skim through eqn 6.25, Ch-§6.3 through 6.3.5 inclusive 8 through 8.2 inclusive 9.1,2	HW 6 Lab 3 (part 2)
8	10/16 10/18	• 2 stage op amp • Common mode and differential gain • RHP zero from compensation cap	Ch-§5.3 (esp. figures §5.23, 5.29 and 5.3)}	Ch-§9.3 through 9.4.3 inclusive	HW 7
9	10/23 10/25	• RHP zero • Current mirror pole/zero doublet • Supply-independent biasing		4.4.2, 4.4.3 biasing; with emphasis on the MOS parts	HW 8 Lab 4
10	10/30 11/01	• Supply and temperature-independent biasing • Midterm review • Midterm 2:			
11	11/06 11/08	• Telescopic and folded cascode • Folded cascode biasing • Switched capacitors, ADCs and DACs • Regulators	Ch-§5.1-5.2 Ch-§9.2	Ch-§6.1.7.1 Switched capacitor amplifier 6.6 folded cascode	HW 9 Lab 5
12	11/13 11/15	• Switched capacitors: ADC, PGA, MOS switch	Ch-§13.2	Ch-§4.2.5.2 high swing current mirrors	Project
13	11/20 11/22	• Rail-to-rail input and output • Rin, Rout, and feedback noise			
14	11/27 11/29	Thanksgiving Break			
15	12/04 12/06	• Op amps: input offset voltage, finite GBW, frequency response in feedback			
16	12/11 12/13	RRR Week Final project presentations			
17	12/16	Final Exam 11:30-14:30 Location TBD			