# EE 140/240A Linear Integrated Circuits
# Fall 2019 Homework 2

## This homework is due September 11, 2019, at 23:00.

**Submission Format**
Your homework submission should consist of **one** file submitted via bCourses.

- `hw2.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

### 1. Good to Know!

Some things you should calculate, some you should just know. I won't let you use calculators on the exams.

(a) Look up the values for Boltzmann's constant and the charge on the electron, and show that $\frac{k_B}{q} \approx 86\frac{\mu V}{K}$ That's a number that you should memorize.

(b) 300K is a little warm for room temperature (it's over 80°F, which may actually be the room temperature in our classroom). For reasonable values of "room temperature", the thermal voltage $V_{TH}$ is either 25mV or 26mV. Pick one of those and memorize it.

**Without using a calculator:**

i. Regardless of the current temperature, how much does the thermal voltage change when the temperature goes up by 1 degree Centigrade?

ii. How much does the thermal voltage change if the temperature goes from 20°C to 70°C (upper bound temp requirement for consumer electronics)?

(c) At "room temperature", calculate $V_{TH} \cdot \ln(10)$. Whatever you came up with, remember the phrase "60 millivolts per decade". It comes up a lot.

### 2. PN Junction Basics

You have a PN junction with $N_D = 10^{18}\text{cm}^{-3}$ and $N_A = 10^{15}\text{cm}^{-3}$. You calculate that the depletion width is about 1μm.

(a) Is the depletion region mostly in the *p*-doped or the *n*-doped side?

(b) Estimate the built-in potential at room temperature without using a calculator. (Hint: your answer should be a multiple of 60mV)

(c) If you increase the $N$ doping by a factor of 10:

i. How much does the built in potential change?

ii. Roughly how much does the depletion width change? (e.g. increase by 10×, decrease by $\sqrt{10}$, slight increase, no change, etc.)

(d) Answer the same questions as part (c), but instead increasing the $P$ doping by a factor of 10.

(e) You apply a reverse bias equal to the built-in potential. Without using a calculator, how much does the depletion region change?

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(f) You apply a reverse bias that causes the depletion region to double from the unbiased state. Without using a calculator, find the junction potential (sum of built-in and the reverse bias) and the applied reverse bias.

## 3. Diode Configurations

You have an array of identical diodes on a silicon chip. They all have a forward voltage of 600mV with a current of 10μA.

(a) If you pass 10μA through a series connected array of 10 diodes, what voltage do you measure?

(b) If you pass 10μA through a parallel connected array of 10 diodes, what voltage do you measure?

(c) If you apply 600mV to a series connection of 2 diodes, what current do you measure? (Hint: Estimate $I_S$)

(d) If you apply 600mV to a parallel connection of 2 diodes, what current do you measure?

(e) If you apply $-600$mV to a single diode, roughly what current do you measure? (Hint: The answer is not 0! Estimate $I_S$)

## 4. BJT Behavior

In an NPN transistor in the forward active region of operation:

(a) Collector current increases with increasing $V_{BE}$ bias because: (your answer should say something about either $n$ or $p$ type carriers, and drift/diffusion currents)

(b) Collector current increases with increasing $V_{CE}$ because: (your answer should say something about what is happening in the base, and how that relates to either $n$ or $p$ type carriers, and either diffusion or drift)

## 5. MOSFET Behavior

In an NMOS transistor in saturation,

(a) Drain current increases with increasing $V_{GS}$ because: (your answer should say something about $n$ or $p$ type carriers, and why there is more or less of them)

(b) Drain current increases with increasing $V_{DS}$ because: (your answer should say something about what is happening in the channel, and how that relates to either $n$ or $p$ type carriers, and either diffusion or drift)

## 6. MOSFET Gate Charge Balancing

In a PMOS device, the charge on the gate is balanced by what types of charges (electrons, holes, positive or negative ions) in these regions of bias:

(a) accumulation

(b) subthreshold

(c) inversion

## 7. MOSFET Regions of Operation

For a 1μm NMOS transistor with $V_{\text{tn}} = 1$V in a circuit with $V_{DD} = 3$V, sketch the regions of operation in a figure with $V_{DS}$ on the horizontal axis and $V_{GS}$ on the vertical axis. Label where the device is OFF, TRIODE, SAT, and SUB-Vt. Draw a dotted line and label the quadratic and velocity saturated regions.

## 8. PMD3001

Real devices do not always fit our simple models very well. The PMD3001 has an NPN and PNP bipolar transistor in the same package. Use the datasheet to answer these questions: https://assets.nexperia.com/documents/data-sheet/PMD3001D.pdf

(a) Looking at Figure 6, estimate the NPN output resistance $r_o$ and Early voltage $V_A$ when
   i. $I_C = 0.8\text{A}$ and $I_B = 3.4\text{mA}$
   ii. $I_B = 1.7\text{mA}$ and $V_{CE} > 2\text{V}$

(b) Looking at Figure 7, near room temperature there is a fairly straight line relating $V_{BE}$ to $I_C$ over three decades of collector current from 0.1mA to 100mA.
   i. What does our theoretical model say the slope of that line should be?
   ii. What is it in the figure?

(c) Also in Figure 7:
   i. The slopes are different at different temperatures. Why? Are they consistent with our model?
   ii. For a fixed collector current, the base-emitter voltage decreases with temperature. Why?
   iii. At $V_{BE} = 0.7\text{V}$, how much does the collector current change from $-55°\text{C}$ to $25°\text{C}$? What does that say about the change in $I_S$?

## 9. 2N7002P

The 2N7002P is a discrete NMOS transistor that costs \$0.017 in volume on digikey.com. https://assets.nexperia.com/documents/data-sheet/2N7002P.pdf

(a) From Figure 6, estimate the threshold voltage and the transconductance (saturation) when $V_{GS} = 2.5\text{V}$. Can you estimate the output resistance when $V_{DS} = V_{GS} = 3\text{V}$? Why or why not?

(b) From Figure 7, estimate the typical sub-threshold slope and the value of the parameter $n$.

## 10. Intel FINFET

Look at the 2014 paper on the Intel 14nm FINFET: https://people.eecs.berkeley.edu/~pister/140sp16/resources/Intel14nmIEDM2014.pdf

(a) From Figure 5, estimate $g_m$, $r_o$, and intrinsic gain for NMOS and PMOS transistors when $V_{GS} = 0.5\text{V}$ and $V_{DS} = 0.5\text{V}$ (PMOS values are negative). Note: the vertical axis in Figure 5 is mislabeled! It should be $\frac{\text{mA}}{\mu\text{m}}$, not $\frac{\text{A}}{\mu\text{m}}$. Figure 6 is correct.

(b) From Figure 5, estimate the threshold voltage for NMOS and PMOS devices. Do these devices look exponential, quadratic, or velocity saturated? Why?

(c) From Figure 6, estimate the subthreshold slope and the parameter $n$ for NMOS and PMOS devices.

## 11. Drain Current vs. Drain and Gate Voltages

(a) Carefully sketch by hand the drain current vs. $V_{DS} \in [0,3]\text{V}$ at a constant $V_{GS} \in \{0,1,2,3\}\text{V}$ for an NMOS transistor with $\frac{W}{L} = \frac{10\mu\text{m}}{1\mu\text{m}}$, $\mu_n C_{ox} = 100\frac{\mu\text{A}}{\text{V}^2}$, $V_{DD} = 3\text{V}$, $\lambda = \frac{1}{10\text{V}}$, and $V_{tn} = 1\text{V}$.

(b) Do the same for a PMOS transistor of the same size with the same parameters except $V_{DS} \in [-3,0]\text{V}$ and $V_{tp} = -1\text{V}$. You should get exactly the same plot as in part (a), but rotated 180 degrees and with different axis labels.

(c) **(EE240A)** Find at least two recent research papers on interesting transistors and calculate intrinsic gain. e.g. nanotubes, graphene, WS2, 7nm, organic, etc.