EE 140/240A Linear Integrated Circuits
Fall 2019 Homework 2

This homework is due September 11, 2019, at 23:00.

Submission Format
Your homework submission should consist of **one** file submitted via bCourses.

- `hw2.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

1. Good to Know!

Some things you should calculate, some you should just know. I won't let you use calculators on the exams.

(a) Look up the values for Boltzmann's constant and the charge on the electron, and show that $\frac{k_B}{q} \approx 86\frac{\mu V}{K}$ That's a number that you should memorize.

Solution:

$$k_B \approx 1.38 \cdot 10^{-23}\frac{J}{K} \approx 8.617 \cdot 10^{-5}\frac{eV}{K}$$

$$q \approx 1.602 \cdot 10^{-19} C$$

$$\frac{k_B}{q} \approx 8.617 \cdot 10^{-5}\frac{V}{K} = 86.17\frac{\mu V}{K}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

(b) 300K is a little warm for room temperature (it's over 80°F, which may actually be the room temperature in our classroom). For reasonable values of "room temperature", the thermal voltage V_{TH} is either 25mV or 26mV. Pick one of those and memorize it.

Without using a calculator:

i. Regardless of the current temperature, how much does the thermal voltage change when the temperature goes up by 1 degree Centigrade?
Solution: From part (a),

$$86.17\mu V$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

ii. How much does the thermal voltage change if the temperature goes from 20°C to 70°C (upper bound temp requirement for consumer electronics)?
Solution: Again using our equation from part (a)

$$\begin{aligned}\Delta V_{\text{TH}} &= 50 \cdot 86\mu\text{V} \\ &= 4.3\text{mV}\end{aligned}$$

$$\Delta V_{\text{TH}} \approx 4.3\text{mV}$$

Rubric: (2 Points)
- +1: Correct equation
- +1: Correct numerical calculation

(c) At "room temperature", calculate $V_{\text{TH}} \cdot \ln(10)$. Whatever you came up with, remember the phrase "60 millivolts per decade". It comes up a lot.
Solution: Using the 26mV value for V_{TH} at room temperature,

$$V_{\text{TH}} \cdot \ln(10) \approx 26\text{mV} \cdot 2.3 \approx 60\text{mV}$$

$$V_{\text{TH,300K}} \approx 60\text{mV}$$

Rubric: (2 Points)
- +1: Correct equation
- +1: Correct numerical calculation

2. PN Junction Basics

You have a PN junction with $N_D = 10^{18}\text{cm}^{-3}$ and $N_A = 10^{15}\text{cm}^{-3}$. You calculate that the depletion width is about 1µm.

(a) Is the depletion region mostly in the p-doped or the n-doped side?
Solution: $N_D \gg N_A$ by three orders of magnitude, so the depletion region is mostly in the p-doped side. The relevant equations:

$$W_{p0} = \left(\frac{2\varepsilon\Psi_0}{qN_A\left(1+\frac{N_A}{N_D}\right)} \right)^{\frac{1}{2}} \qquad W_{n0} = \left(\frac{2\varepsilon\Psi_0}{qN_D\left(1+\frac{N_D}{N_A}\right)} \right)^{\frac{1}{2}}$$

The p-doped side of the depletion region is wider

Rubric: (1 Points)

- +1: Correctly identify region

(b) Estimate the built-in potential at room temperature without using a calculator. (Hint: your answer should be a multiple of 60mV)

Solution: Using our equation for the built-in potential:

$$\begin{aligned}\phi_0 &= V_{\text{TH}} \ln\left(\frac{N_D N_A}{n_i^2}\right)\\ &= 13 V_{\text{TH}} \ln(10)\\ &\approx 13 \times 60\text{mV}\\ &\approx 0.78\text{V}\end{aligned}$$

$$\phi_0 \approx 0.78\text{V}$$

Rubric: (1 Points)

- +1: Correct equation and numerical value

(c) If you increase the N doping by a factor of 10:

i. How much does the built in potential change?

Solution: Looking to the equation

$$\phi_0 = V_{\text{TH}} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

it changes by $+V_{\text{TH}} \ln(10) \approx 60\text{mV}$

60mV

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

ii. Roughly how much does the depletion width change? (e.g. increase by $10\times$, decrease by $\sqrt{10}$, slight increase, no change, etc.)

Solution: Looking to our equations for a PN junction under zero bias:

$$\begin{aligned}W_0 &= W_{p0} + W_{n0}\\ &= \left(\frac{2\varepsilon\Psi_0}{qN_A\left(1+\frac{N_A}{N_D}\right)}\right)^{\frac{1}{2}} + \left(\frac{2\varepsilon\Psi_0}{qN_D\left(1+\frac{N_D}{N_A}\right)}\right)^{\frac{1}{2}}\end{aligned}$$

Modifying the n doping has very marginal change in the total depletion width since the majority of the depletion width is contained in the p-doped side.

Small change

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct conclusion for small change

(d) Answer the same questions as part (c), but instead increasing the P doping by a factor of 10.

Solution: For the built-in potential, it once again changes by ≈ 60mV

$$\Delta\phi_0 \approx 60\text{mV}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

And now once again looking to the equations in part (c) (and also recognizing that the majority of the depletion width falls on the p-doped side and so $W_{p0} \gg W_{n0}$)

Decrease by a factor of roughly $\sqrt{10}$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

(e) You apply a reverse bias equal to the built-in potential. Without using a calculator, how much does the depletion region change?

Solution: As a function of forward bias V_D,

$$W(V_D) = W_0\sqrt{1-\frac{V_D}{\phi_0}}$$

where W_0 is the zero-bias depletion region width. For reverse bias, the depletion width would increase by a factor of $\sqrt{2}$

Increase by a factor of $\sqrt{2}$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

(f) You apply a reverse bias that causes the depletion region to double from the unbiased state. Without using a calculator, find the junction potential (sum of built-in and the reverse bias) and the applied reverse bias.

Solution: Referring to the equation relating forward bias voltage to depletion region width:

$$W(V_D) = W_0\sqrt{1-\frac{V_D}{\phi_0}}$$

Increasing the depletion region to twice its original width requires a reverse bias of $3\phi_0$. Finding the junction potential

$$\phi_j = \phi_0 + 3\phi_0 \approx 3.12\text{V}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

3. Diode Configurations

You have an array of identical diodes on a silicon chip. They all have a forward voltage of 600mV with a current of 10µA.

(a) If you pass 10µA through a series connected array of 10 diodes, what voltage do you measure?
Solution:

$$600\text{mV} \cdot 10 = 6\text{V}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

(b) If you pass 10µA through a parallel connected array of 10 diodes, what voltage do you measure
Solution: Each diode in the array of 10 parallel diodes would conduct $\frac{10\mu\text{A}}{10} = 1\mu\text{A}$.
Looking to our equation relating voltage and current through a diode:

$$I_D(V_D) = I_S \cdot \left[\exp\left(\frac{V_D}{n}\frac{q}{k_B T}\right) - 1\right]$$
$$V_D(I_D) = n\frac{k_B T}{q}\ln\left(1 + \frac{I_D}{I_S}\right)$$

where n is an ideality factor which for the purposes of this problem is 1. In the forward bias region where typically $I_D \gg I_S$, a decade decrease in I_D (like 10µA to 1µA) decreases the forward voltage by 60mV

$$600\text{mV} - 60\text{mV} = 540\text{mV}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

(c) If you apply 600mV to a series connection of 2 diodes, what current do you measure? (Hint: Estimate I_S)
Solution:

$$V_D = 300\text{mV} = 600\text{mV} - 5 \times 60\text{mV}$$

and given the rule of 60mV per decade, that gives you 5 decades' less current

$$I_D \approx 100\text{pA}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

(d) If you apply 600mV to a parallel connection of 2 diodes, what current do you measure?
Solution:

$$10\mu\text{A} \cdot 2 = 20\mu\text{A}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

(e) If you apply -600mV to a single diode, roughly what current do you measure? (Hint: The answer is not 0! Estimate I_S)
Solution: Looking once more to the diode equation

$$I_D = I_S \left(\exp\left(\frac{V_D}{V_{TH}} \right) - 1 \right)$$

the exponential is extremely small relative to 1, so the current magnitude is roughly I_S, which we can estimate based on 600mV = $10\times$ 60mV, so I_D at 600mV is ten orders of magnitude larger than I_S, therefore

$$I_S \approx 100\text{fA}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical calculation

4. BJT Behavior

In an NPN transistor in the forward active region of operation:

(a) Collector current increases with increasing V_{BE} bias because: (your answer should say something about either n or p type carriers, and drift/diffusion currents)
Solution:

n-type carriers diffuse across the emitter-base junction when the junction is forward biased. The diffusion current is exponential in the forward bias voltage.

Rubric: (2 Points)

- +1: N-type carriers only (no mention of p-type). It's okay to say that increasing the forward bias lowers the potential barrier for electrons being injected into the base, or that it decreases the electric field in the depletion region.
- +1: Diffusion current only (no mention of drift).

(b) Collector current increases with increasing V_{CE} because: (your answer should say something about what is happening in the base, and how that relates to either n or p type carriers, and either diffusion or drift)

Solution:

> Incresing V_{CE} increases the width of the collector-base depletion region in the base, which decreases the base width. This increases the concentration gradient of n-type carriers in the base, which increases the diffusion current of n-type carriers through the base.

Rubric: (2 Points)

- +1: N-type carriers only (no mention of p-type carriers)
- +1: Diffusion current only (no mention of drift or electric field).

5. MOSFET Behavior

In an NMOS transistor in saturation,

(a) Drain current increases with increasing V_{GS} because: (your answer should say something about n or p type carriers, and why there is more or less of them)

Solution:

> Increasing the gate voltage increases the density of n-type carriers by attracting more of them to for a strong channel between source and drain.

Rubric: (2 Points)

- +2: If the arguments are close to the solution

(b) Drain current increases with increasing V_{DS} because: (your answer should say something about what is happening in the channel, and how that relates to either n or p type carriers, and either diffusion or drift)

Solution:

> Increasing V_{DS} increases drain current (drift, electrons) at least in part due to channel length modulation—the channel length effectively decreases in length. The shorter the channel, the greater the fraction of the initial channel length the modulation consumes.

Rubric: (2 Points)

- +2: If the arguments are close to the solution

6. MOSFET Gate Charge Balancing

In a PMOS device, the charge on the gate is balanced by what types of charges (electrons, holes, positive or negative ions) in these regions of bias:

(a) accumulation

Solution:

holes and fixed positive ions

Rubric: (2 Points)

- +2: Correct

(b) subthreshold

Solution:

Fixed positive ions and nearly depleted minority carriers' holes

Rubric: (2 Points)

- +2: Correct

(c) inversion

Solution:

Minority carriers, holes form an inversion layer, fixed positive ions

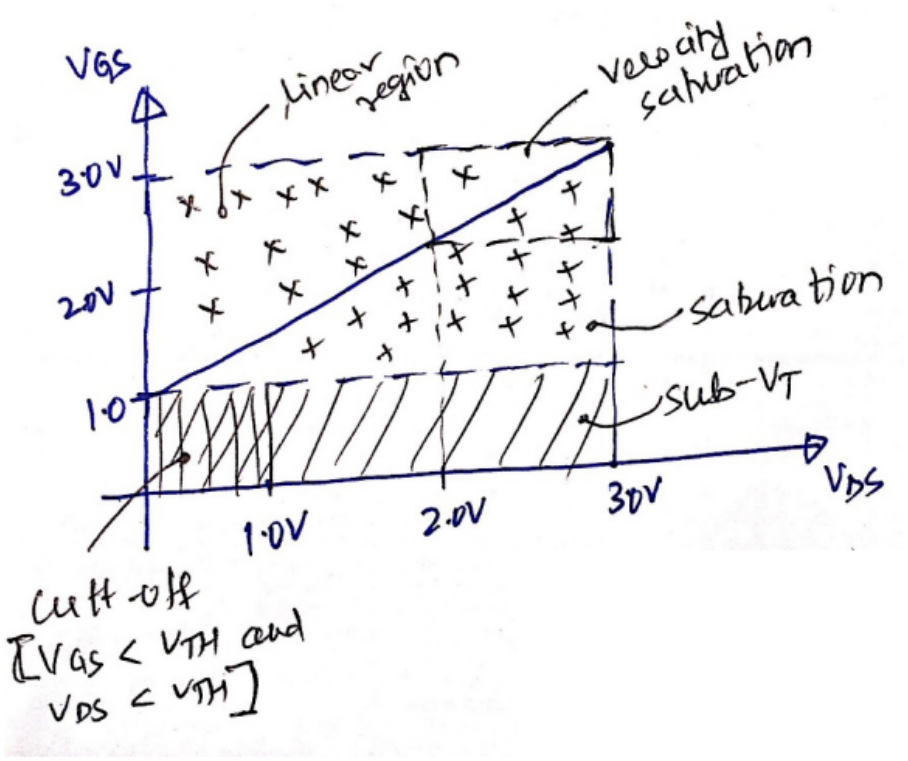
Rubric: (2 Points)

- +2: Correct

7. MOSFET Regions of Operation

For a 1µm NMOS transistor with $V_{\text{tn}} = 1\text{V}$ in a circuit with $V_{DD} = 3\text{V}$, sketch the regions of operation in a figure with V_{DS} on the horizontal axis and V_{GS} on the vertical axis. Label where the device is OFF, TRIODE, SAT, and SUB-Vt. Draw a dotted line and label the quadratic and velocity saturated regions.

Solution:



Rubric: (10 Points)

- +2: Identify cutoff
- +2: Identify subthreshold
- +2: Identify linear region
- +2: Identify quadratic saturation region
- +2: Identify velocity saturation region

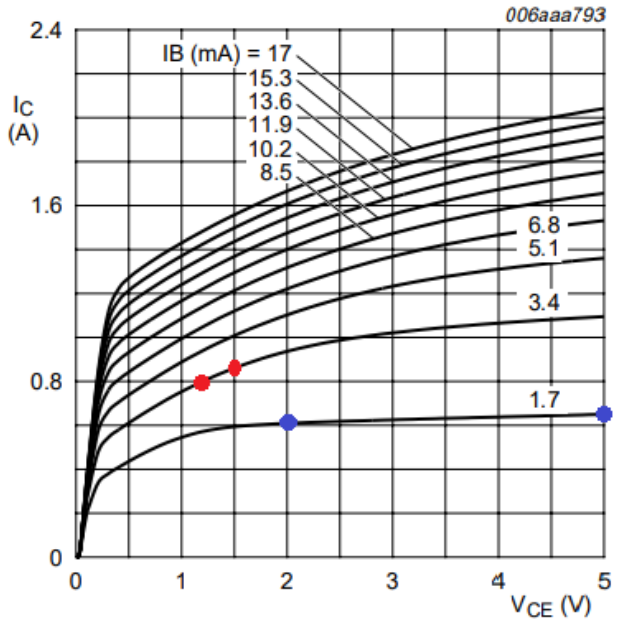
8. PMD3001

Real devices do not always fit our simple models very well. The PMD3001 has an NPN and PNP bipolar transistor in the same package. Use the datasheet to answer these questions: https://assets.nexperia.com/documents/data-sheet/PMD3001D.pdf

(a) Looking at Figure 6, estimate the NPN output resistance r_o and Early voltage V_A when

i. $I_C = 0.8\text{A}$ and $I_B = 3.4\text{mA}$

Solution:



To calculate r_o and V_A, we use the red dots.

$$r_o = \frac{dV_{ce}}{dI_C}$$

$$V_A = r_o I_C$$

$$r_o \approx 5\Omega$$

$$V_A \approx 4.0\text{V}$$

Rubric: (3 Points)

- +2: Correct equation
- +1: Roughly correct numerical value

ii. $I_B = 1.7\text{mA}$ and $V_{CE} > 2\text{V}$

Solution: Using the blue dots,

$$\begin{aligned} r_o &= \frac{dV_{ce}}{dI_C} \\ &\approx \frac{5-2}{0.65-0.6}\frac{\text{V}}{\text{A}} \\ &= 60\Omega \\ V_A &= r_o I_C \\ &\approx 36\text{V} \end{aligned}$$

$$r_o \approx 60\Omega$$

$$V_A \approx 36\text{V}$$

Rubric: (3 Points)

- +2: Correct equation
- +1: Roughly correct numerical value

(b) Looking at Figure 7, near room temperature there is a fairly straight line relating V_{BE} to I_C over three decades of collector current from 0.1mA to 100mA.

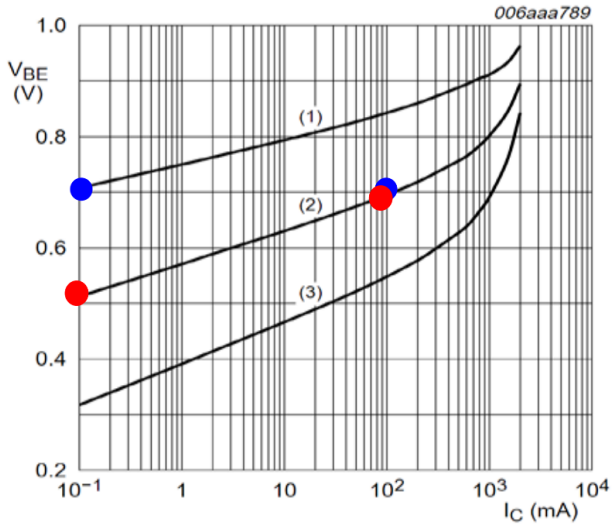
i. What does our theoretical model say the slope of that line should be?
Solution:

60mV/decade

Rubric: (1 Points)

- +1: Correct value

ii. What is it in the figure?
Solution:



Using the red dots,

$\approx$ 60mV/decade

Rubric: (3 Points)

- +2: Correct equation
- +1: Correct numerical value

(c) Also in Figure 7:

i. The slopes are different at different temperatures. Why? Are they consistent with our model?
Solution:

The slopes vary with temperature, which is consistent with our model since V_{TH} varies with temperature.

Rubric: (1 Points)

- +2: Correct argument

ii. For a fixed collector current, the base-emitter voltage decreases with temperature. Why?
Solution:

The base-emitter junction is a diode, and as such will have a negative tempreature coefficient given a fixed current. Although V_{TH} increases linearly with temperature, I_S (even with the logarithm) increases much faster with temperature, resulting in an overall negative temperature coefficient.

Rubric: (4 Points)
- +4: Correct argument

iii. At $V_{BE} = 0.7$V, how much does the collector current change from $-55°$C to $25°$C? What does that say about the change in I_S?
Solution:

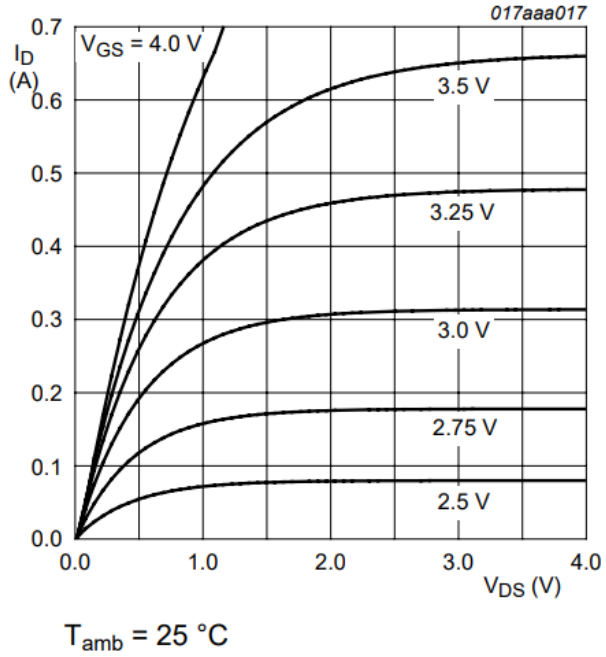
For $V_{BE} = 0.7$V, I_C changes from 0.1mA to 100mA (marked with the blue dots). This is primarily due to a change in I_S, which supports our claim that I_S is very temperature sensitive.

Rubric: (4 Points)
- +2: Roughly correct value of I_C
- +2: Correct argument

9. 2N7002P

The 2N7002P is a discrete NMOS transistor that costs \$0.017 in volume on digikey.com. https://assets.nexperia.com/documents/data-sheet/2N7002P.pdf

(a) From Figure 6, estimate the threshold voltage and the transconductance (saturation) when $V_{GS} = 2.5$V. Can you estimate the output resistance when $V_{DS} = V_{GS} = 3$V? Why or why not?
Solution:



At $V_{GS} = 2.5\text{V}$, it appears as though the device enters saturation when $V_{DS} \approx 1\text{V}$, so $V_{GS} - V_t = 1\text{V}$. Note that this roughly matches the value for the threshold voltage provided by the datasheet.

For calculating transconductance in saturation,

$$g_m = \frac{2I_D}{V_{ov}} \approx 2\frac{0.08\text{A}}{1\text{V}} = 0.16\text{S}$$

$$V_t \approx 1.5\text{V}$$

$$g_m \approx 0.16\text{S}$$

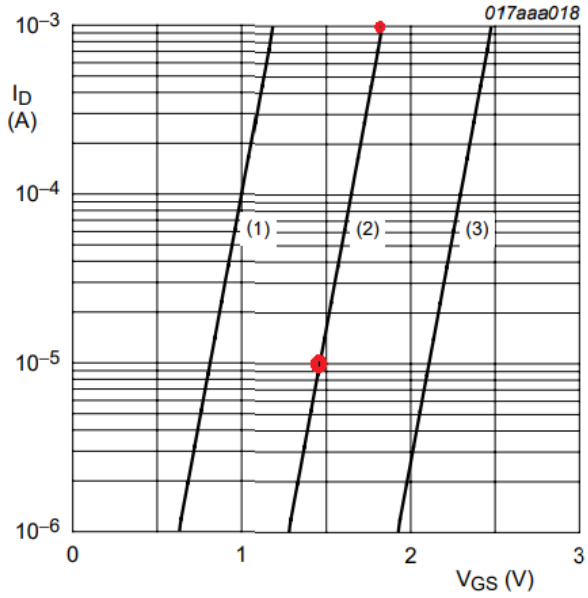
As it appears in the figure, the output resistance is very high. We could measure it from the graph, but likely it would be highly inaccurate.

Rubric: (5 Points)

- +2: V_{TH} calculation
- +2: Correct process for g_m calculation
- +1: Correct process for r_o calculation

(b) From Figure 7, estimate the typical sub-threshold slope and the value of the parameter n.

Solution:



T_{amb} = 25 °C; V_{DS} = 5 V
(1) minimum values
(2) typical values
(3) maximum values

Using the red dots,

$$S \approx \frac{1.7 - 1.59}{2} \approx 100\text{mV/decade}$$

And from that we use

$$n = \frac{S}{60\text{mV/decade}}$$

$$S \approx 100\text{mV/decade}$$
$$n \approx 1.67$$

Rubric: (4 Points)

- +2: Correct process for calculating S
- +2: Correct process for calculating n

10. Intel FINFET

Look at the 2014 paper on the Intel 14nm FINFET: https://people.eecs.berkeley.edu/~pister/140sp16/resources/Intel14nmIEDM2014.pdf

(a) From Figure 5, estimate g_m, r_o, and intrinsic gain for NMOS and PMOS transistors when $V_{GS} = 0.5\text{V}$ and $V_{DS} = 0.5\text{V}$ (PMOS values are negative). Note: the vertical axis in Figure 5 is mislabeled! It should be $\frac{\text{mA}}{\mu\text{m}}$, not $\frac{\text{A}}{\mu\text{m}}$. Figure 6 is correct.

Solution:

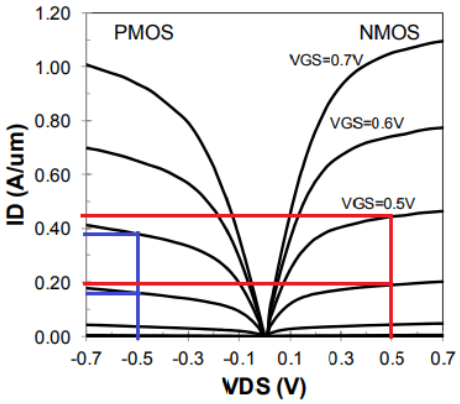


Figure 5: Transistor I-V Curves

Using the red lines for NMOS and blue lines for PMOS,

$$\begin{aligned} g_{m,n} &= \frac{dI_D}{d_{V_{GS}}} \\ &= \frac{0.4 - 0.2\text{mA/}\mu\text{m}}{0.5 - 0.4\text{V}} \\ &= 2\text{mS/}\mu\text{m} \end{aligned}$$

$$\begin{aligned} r_{o,n} &= \frac{dV_{DS}}{dI_D} \\ &= \frac{0.7 - 0.3\text{V}}{0.5 - 0.4\text{mA/}\mu\text{m}} \\ &= 4\text{k}\Omega \cdot \mu\text{m} \end{aligned}$$

$$\begin{aligned} A_{v0,n} &= -g_{m,n} r_{o,n} \\ &= -8 \end{aligned}$$

$$g_{m,p} = \frac{dI_D}{d_{V_{GS}}} = \frac{0.38 - 0.15\text{mA}/\mu\text{m}}{0.5 - 0.4\text{V}} = 2.3\text{mS} \cdot \mu\text{m}$$

$$r_{o,p} = \frac{dV_{DS}}{dI_D} = \frac{0.7 - 0.3\text{V}}{0.4 - 0.3\text{mA}/\mu\text{m}} = 4\text{k}\Omega/\mu\text{m}$$

$$A_{vo,p} = -g_{m,p} r_{o,p} = -9.2$$

	g_m	r_o	A_{v0}
NMOS	$2\text{mS}/\mu\text{m}$	$4\text{k}\Omega \cdot \mu\text{m}$	-8
PMOS	$2.3\text{mS}/\mu\text{m}$	$4\text{k}\Omega \cdot \mu\text{m}$	-9.2

Rubric: (4 Points)

- +1: Correct g_m for NMOS and PMOS ($2\times$)
- +1: Correct r_o for NMOS and PMOS ($2\times$)

(b) From Figure 5, estimate the threshold voltage for NMOS and PMOS devices. Do these devices look exponential, quadratic, or velocity saturated? Why?

Solution: Finding the threshold, take $V_{DS} = 0.2\text{V}, V_{GS} = 0.5\text{V} \longrightarrow V_{tn} = 0.3\text{V}$ and the same for the PMOS $V_{SD} = 0.25\text{V}, V_{SG} = 0.5\text{V} \longrightarrow V_{tp} = 0.25\text{volt}$.

$$V_{tn} \approx 0.3\text{V}$$

$$V_{tp} \approx 0.25\text{V}$$

Referring to the figure above, the devices have both saturation and velocity saturation regions depending on the value of V_{GS}. For $V_{GS} = 0.3\text{V}$ to 0.5V, the overdrive increase by $3\times$ and the current increases by $9\times$, indicating quadratic behavior. However, for $V_{GS} > 0.5\text{V}$, the drain current only increases linearly, indicating velocity saturation.

Rubric: (4 Points)

- +1: Correct threshold voltage for NMOS and PMOS ($2\times$)
- +1: Check for quadratic behavior for NMOS and PMOS ($2\times$)

(c) From Figure 6, estimate the subthreshold slope and the parameter n for NMOS and PMOS devices.

Solution:

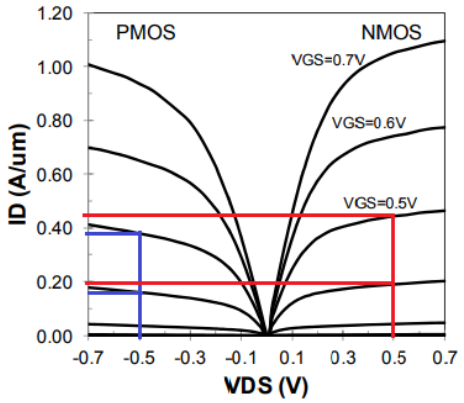


Figure 5: Transistor I-V Curves

Device	S	n
hline NMOS	70mV/dec	1.2
PMOS	70mV/dec	1.2

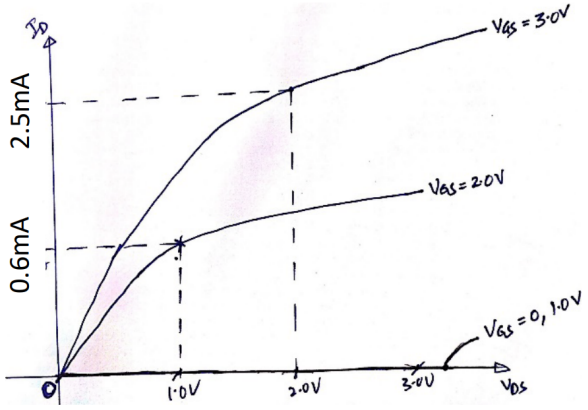
Rubric: (4 Points)

- +1: Correct subthreshold slope for NMOS and PMOS (2×)
- +1: Correct n for NMOS and PMOS (2×)

11. Drain Current vs. Drain and Gate Voltages

(a) Carefully sketch by hand the drain current vs. $V_{DS} \in [0,3]$V at a constant $V_{GS} \in \{0,1,2,3\}$V for an NMOS transistor with $\frac{W}{L} = \frac{10\mu m}{1\mu m}$, $\mu_n C_{ox} = 100\frac{\mu A}{V^2}$, $V_{DD} = 3$V, $\lambda = \frac{1}{10V}$, and $V_{tn} = 1$V.

Solution:

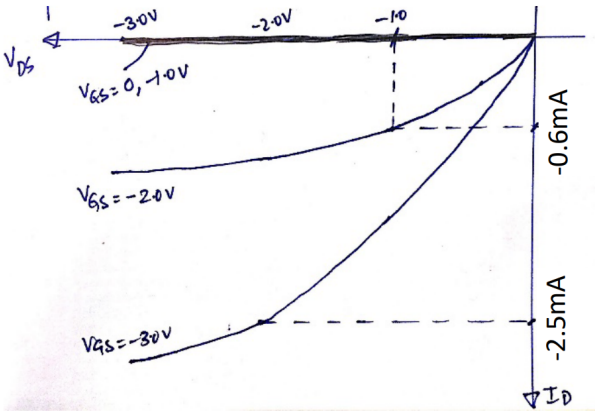


Rubric: (5 Points)

- +2: Shape of I_D vs. V_{DS} plot
- +3: Correct values

(b) Do the same for a PMOS transistor of the same size with the same parameters except $V_{DS} \in [-3, 0]$V and $V_{tp} = -1$V. You should get exactly the same plot as in part **??**, but rotated 180 degrees and with different axis labels.

Solution:



Rubric: (5 Points)

- +2: Shape of I_D vs. V_{DS} plot
- +3: Correct values

(c) **(EE240A)** Find at least two recent research papers on interesting transistors and calculate intrinsic gain. e.g. nanotubes, graphene, WS2, 7nm, organic, etc.

Solution: Up to you!

Rubric: (2 Points)

- +1: Good faith effort
- +1: Correct equations used