EE 140/240A Linear Integrated Circuits
Fall 2019 Homework 4

This homework is due September 25, 2019, at 23:00.

Submission Format

Your homework submission should consist of **one** file.

- `hw4.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit each file to its respective assignment on bCourses.

1. Single-Pole Amplifier (Spring 2015 Midterm 1 Q1)

Fill in the following table where each row is a different single-pole amplifier.

G_m (S)	R_o (Ω)	C_L (F)	$\lvert A_{v0}\rvert$ (V/V)	ω_p (rad/s)	ω_u (rad/s)
10m			10		100G
1µ	1M	10f			
		1p	100	10M	

2. New Transistor, Who Dis (Spring 2015 Midterm 1 Q3b)

You invent a new transistor and find the output current is given by

$$I_{xy} = KV_{zy}^3 V_{xy}^{\frac{1}{2}}$$
$$I_z = 0$$

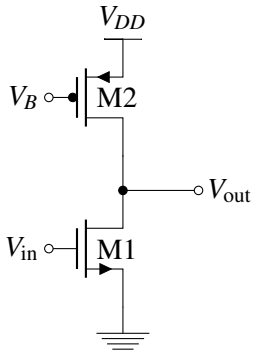
(a) What are the formulas for transconductance and output resistance?

(b) What is the intrinsic gain when the device is biased at $V_{zy} = V_{xy} = 1\text{V}$? Give a numerical answer.

3. (Spring 2015 Midterm 1 Q4)

You have biased the amplifier below with a particular input overdrive voltage V_{ov}. Both devices are in saturation, and the quadratic model is appropriate.

The low frequency gain is $-1000\frac{\text{V}}{\text{V}}$. $C_{gs1} = 1\text{pF}, C_{gd1} = 0.1\text{pF}$.



(a) What is the input capacitance? Give an exact numerical answer.

(b) You adjust the bias voltages so that the input overdrive V_{ov1} **increases by a factor of two**. What happens to the current, small signal parameters, low frequency gain, output pole frequency, output unity gain frequency, and input capacitance? Answers should be in the form "increase 5×", "decrease 10×", "stay the same", etc.

I_D	
g_m	
r_o	
$\lvert A_{v0}\rvert$	
ω_p	
ω_u	
C_{in}	

4. RC Low-Pass Filters

An RC low pass filter has a time constant of 1µs.

(a) With an input of $1\text{V} \cdot \sin(10^7 \frac{\text{rad}}{\text{s}} \cdot t)$, draw one cycle of the input and the steady state output. Label the amplitude and phase of the output.

(b) Draw the response to a unit step voltage on a time scale of 1ms, 1µs, and 1ns.

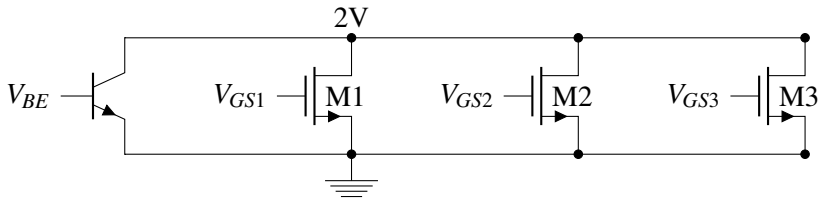
5. (Spring 2016 Midterm 1 Q6)

The four transistors shown below are all biased at a current of 1µA at room temperature.

The NMOS device M1 is in sub-threshold, with $V_{GS} - V_t = -200\text{mV}$ and $n = 1.5$.

The NMOS device M2 is velocity saturated with $V_{GS} - V_t = 100\text{mV}$.

The NMOS device M3 is in saturation, with a channel field of approximately $0.1\text{V}/\mu\text{m}$ and $V_{GS} - V_t = 100\text{mV}$.



(a) Approximately what change in V_{BE} will cause the collector current to increase by a factor of 10?

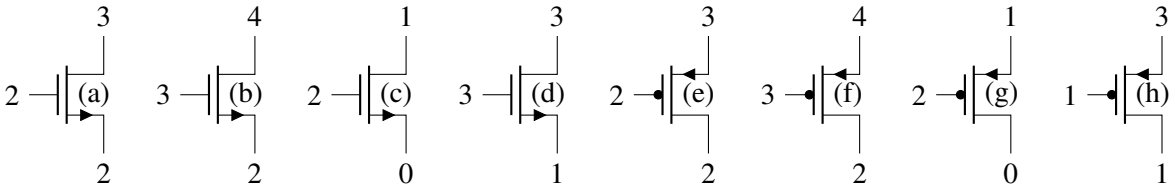
(b) Approximately what change in V_{GS1} will cause the drain current in M1 to increase by a factor of 10?

(c) Approximately what change in V_{GS2} will cause the drain current in M2 to increase by a factor of 10?

(d) Approximately what change in V_{GS3} will cause the drain current in M3 to increase by a factor of 10?

6. (Fall 2009 Midterm 1 Q1)

For the following problems, the drain, gate, and source voltages are given. You may assume $V_{SB} = 0$V and that $V_{tn} = -V_{tp} = 0.5$V. Indicate if the devices are off, in the linear or triode region, or in saturation. If the devices are in saturation, calculate $|V_{dsat}|$.



	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)
Off/Lin/Sat								
V_{dsat} (if Sat)								

7. Common Source Amp Design

The parameters for a particular 0.5µm CMOS process are:

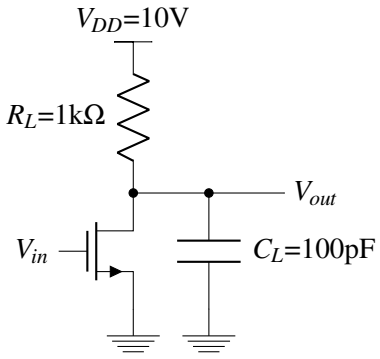
- $C_{ox} = 5\frac{\text{fF}}{\mu\text{m}^2}$
- $C_{ol} = 0.5\frac{\text{fF}}{\mu\text{m}}$
- $\mu_n C_{ox} = 2\mu_p C_{ox} = 200\frac{\mu\text{A}}{\text{V}^2}$
- $\lambda = \frac{1}{10\text{V}}$ when $L = 0.5\mu$m
- $V_{tn} = -V_{tp} = 0.5$V
- $V_{DD} = 2$V

(a) Design an NMOS-input common source amplifier with a PMOS load with a low frequency gain of approximately 200V/V, a unity gain frequency of 1Grad/s with a 1pF load, and an output swing of at least 300mV to 2.2V with a 2.5V single-sided supply. **Minimize power consumption.** Clearly indicate what values you are using for g_m, r_o, I_D, V_{dsat}, gate bias, W, and L for each transistor. Clearly indicate which parameters you "pick", and which you solve for. Calculate the input capacitance.

(b) How much could you change the input capacitance if you were primarily optimizing to minimize that?

8. Common Source With No Calculator

An NMOS common source amplifier has a 10V supply and a 1kΩ load (to the supply) in parallel with 100pF. Assume $\mu_n C_{ox} = 20\mu\text{A/V}^2$, $W/L = 10{,}000/1$, $V_{tn} = 1$V, and $\lambda = 0.01$V. You should be able to do all of the calculations by hand (without calculators). One-ish significant digits is fine.



(a) Write an expression for I_D as a function of output bias point. How much does I_D change as the output voltage varies from 9V to 1V?

(b) What is the change in the input and overdrive voltage as the output varies from 9V to 1V?

(c) Write an expression for g_m and r_o as a function of output bias point.

(d) Write an expression for a_{v0}—the intrinsic gain of the NMOS—as a function of output bias point.

(e) Fill in the following table given the output bias point. Be sure to specify your units!

Output Bias Point	I_D	g_m	r_o	A_{v0}	ω_p	ω_u
9V						
6V						
1V						