EE 140/240A Linear Integrated Circuits
Fall 2019 Homework 4

This homework is due September 25, 2019, at 23:00.

Submission Format

Your homework submission should consist of **one** file.

- `hw4.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit each file to its respective assignment on bCourses.

1. Single-Pole Amplifier (Spring 2015 Midterm 1 Q1)

Fill in the following table where each row is a different single-pole amplifier.

G_m (S)	R_o (Ω)	C_L (F)	$\lvert A_{v0}\rvert$ (V/V)	ω_p (rad/s)	ω_u (rad/s)
10m			10		100G
1µ	1M	10f			
		1p	100	10M	

Solution: Once again for the single-pole amplifier, we have the following equations:

$$A_{v0} = -G_m R_o$$
$$\omega_p = \frac{1}{R_o C_L}$$
$$\omega_u = |A_{v0}|\,\omega_p = \frac{G_m}{C_L}$$

G_m (S)	R_o (Ω)	C_L (F)	$\lvert A_{v0}\rvert$ (V/V)	ω_p (rad/s)	ω_u (rad/s)
10m	**1k**	**100f**	10	**10G**	100G
1µ	1M	10f	**1**	**100M**	**0 to 100M**
1m	**100k**	1p	100	10M	**1G**

Rubric: (18 Points)

- +2: Correct numerical answer. (9×)

2. New Transistor, Who Dis (Spring 2015 Midterm 1 Q3b)

You invent a new transistor and find the output current is given by

$$I_{xy} = K V_{zy}^3 V_{xy}^{\frac{1}{2}}$$
$$I_z = 0$$

(a) What are the formulas for transconductance and output resistance?

Solution: In this, our input is at Z and our output is at X.

$$g_m = \frac{\partial I_{xy}}{\partial V_{zy}} = 3KV_{zy}^2 V_{xy}^{\frac{1}{2}}$$

$$r_o = \left(\frac{\partial I_{xy}}{\partial V_{xy}}\right)^{-1} = \left(\frac{1}{2}KV_{zy}^3 V_{xy}^{-\frac{1}{2}}\right)^{-1} = \frac{2V_{xy}^{\frac{1}{2}}}{KV_{zy}^3}$$

$$g_m = 3KV_{zy}^2 V_{xy}^{\frac{1}{2}}$$

$$r_o = \frac{2V_{xy}^{\frac{1}{2}}}{KV_{zy}^3}$$

Rubric: (4 Points)

- +2: Correct g_m expression
- +2: Correct r_o expression

(b) What is the intrinsic gain when the device is biased at $V_{zy} = V_{xy} = 1\text{V}$? Give a numerical answer.

Solution:

$$A_{v0} = -g_m r_o = -\frac{6V_{xy}}{V_{zy}} = -6\frac{\text{V}}{\text{V}}$$

$$A_{v0} = -6\frac{\text{V}}{\text{V}}$$

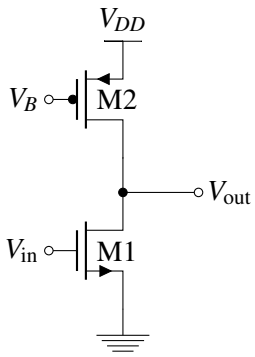
Rubric: (2 Points)

- +1: Correct sign
- +1: Correct magnitude

3. (Spring 2015 Midterm 1 Q4)

You have biased the amplifier below with a particular input overdrive voltage V_{ov}. Both devices are in saturation, and the quadratic model is appropriate.

The low frequency gain is $-1000\frac{\text{V}}{\text{V}}$. $C_{gs1} = 1\text{pF}, C_{gd1} = 0.1\text{pF}$.



(a) What is the input capacitance? Give an exact numerical answer.

Solution: Taking into account the Millerized C_{gd},

$$\begin{aligned} C_{\text{in}} &= C_{gs1} + (1 - A_{v0})C_{gd1} \\ &= 1\text{pF} + (1 + 1000)0.1\text{pF} \\ &= 1\text{pF} + 100.1\text{pF} \\ &= 101.1\text{pF} \end{aligned}$$

$$C_{\text{in}} = 101.1\text{pF}$$

Rubric: (2 Points)

- +1: Correct magnitude
- +1: Correct sign

(b) You adjust the bias voltages so that the input overdrive V_{ov1} **increases by a factor of two**. What happens to the current, small signal parameters, low frequency gain, output pole frequency, output unity gain frequency, and input capacitance? Answers should be in the form "increase 5×", "decrease 10×", "stay the same", etc.

I_D	
g_m	
r_o	
$\lvert A_{v0} \rvert$	
ω_p	
ω_u	
C_{in}	

Solution:

I_D	Increase 4×
g_m	Increase 2×
r_o	Decrease 4×
$\lvert A_{v0}\rvert$	Decrease 2×
ω_p	Increase 4×
ω_u	Increase 2×
C_{in}	Roughly decrease 2×

Rubric: (14 Points)

- +2: Each correct answer (7×)

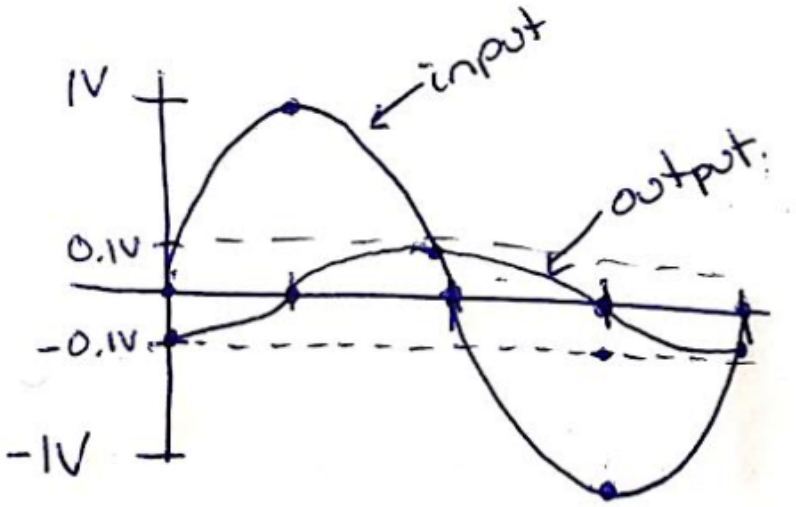
4. RC Low-Pass Filters

An RC low pass filter has a time constant of 1µs.

(a) With an input of $1\text{V} \cdot \sin(10^7 \frac{\text{rad}}{\text{s}} \cdot t)$, draw one cycle of the input and the steady state output. Label the amplitude and phase of the output.

Solution: Note that $\tau = RC$ has units in rad/s, *not* hertz! $\omega_p = \frac{1}{\tau} = 1\frac{\text{Mrad}}{\text{s}}$.

At the pole frequency, the magnitude is divided by $\sqrt{2}$. One decade above the pole frequency, the magnitude is 10× less than the input and the phase is $-90°$ (think back to Bode plots!)

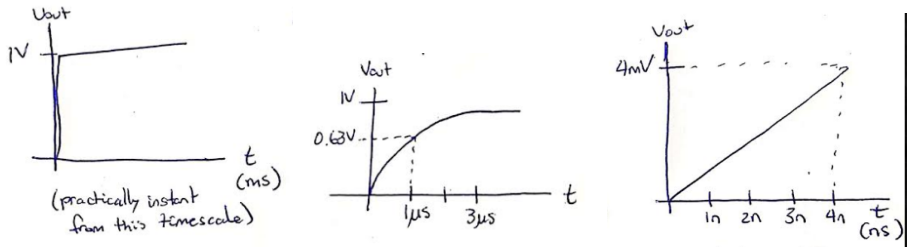


Rubric: (2 Points)

- +1: Correct amplitude
- +1: Correct phase

(b) Draw the response to a unit step voltage on a time scale of 1ms, 1µs, and 1ns.

Solution: Zooming in, things look pretty linear at really small timescales



Rubric: (3 Points)

- +1: Correct error or value for one time scale (3×)

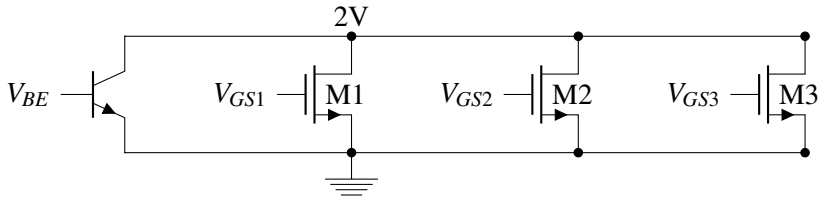
5. (Spring 2016 Midterm 1 Q6)

The four transistors shown below are all biased at a current of 1µA at room temperature.

The NMOS device M1 is in sub-threshold, with $V_{GS} - V_t = -200\text{mV}$ and $n = 1.5$.

The NMOS device M2 is velocity saturated with $V_{GS} - V_t = 100\text{mV}$.

The NMOS device M3 is in saturation, with a channel field of approximately $0.1\text{V}/\mu\text{m}$ and $V_{GS} - V_t = 100\text{mV}$.



(a) Approximately what change in V_{BE} will cause the collector current to increase by a factor of 10?

Solution:

$$\begin{aligned} V_{BE} &\approx \frac{k_B T}{q} \ln\left(\frac{I_E}{I_0}\right) \\ V_{BE} + \Delta V_{BE} &= \frac{k_B T}{q} \ln\left(\frac{10 I_E}{I_0}\right) \\ &= \frac{k_B T}{q} \ln\left(\frac{I_E}{I_0}\right) + \frac{k_B T}{q} \ln(10) \\ &= V_{BE} + \frac{k_B T}{q} \ln(10) \end{aligned}$$

$$\Delta V_{BE} = \frac{k_B T}{q} \approx 60\text{mV}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical value

(b) Approximately what change in V_{GS1} will cause the drain current in M1 to increase by a factor of 10?
Solution:

$$\begin{aligned} I_D &= I_0 \cdot \exp\left(\frac{V_{GS}-V_t}{n}\left(\frac{q}{k_BT}\right)\right) \\ V_{GS}-V_t &= n\frac{k_BT}{q}\ln\left(\frac{I_D}{I_0}\right) \\ V_{GS}+\Delta V_{GS}-V_t &= n\frac{k_BT}{q}\ln\left(\frac{10I_D}{I_0}\right) \\ &= n\frac{k_BT}{q}\ln\left(\frac{I_D}{I_0}\right)+n\frac{k_BT}{q}\ln(10) \\ \Delta V_{GS} &= n\frac{k_BT}{q}\ln(10) \end{aligned}$$

$$\Delta V_{GS} = n\frac{k_BT}{q}\ln(10) \approx 90\text{mV}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical value

(c) Approximately what change in V_{GS2} will cause the drain current in M2 to increase by a factor of 10?
Solution:

$$\begin{aligned} I_D &= C(V_{GS}-V_t) \\ C(V_{GS}+\Delta V_{GS}-V_t) &= 10C(V_{GS}-V_t) \\ \Delta V_{GS} &= 9(V_{GS}-V_t) \end{aligned}$$

$$\Delta V_{GS} = 9(V_{GS}-V_t) = 900\text{mV}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical value

(d) Approximately what change in V_{GS3} will cause the drain current in M3 to increase by a factor of 10?
Solution:

$$\begin{aligned} I_D &= C(V_{GS}-V_t)^2 \\ C(V_{GS}+\Delta V_{GS}-V_t)^2 &= 10C(V_{GS}-V_t)^2 \\ V_{GS}+\Delta V_{GS}-V_t &= \sqrt{10}\,(V_{GS}-V_t) \\ \Delta V_{GS} &= (V_{GS}-V_t)\left(\sqrt{10}-1\right) \end{aligned}$$

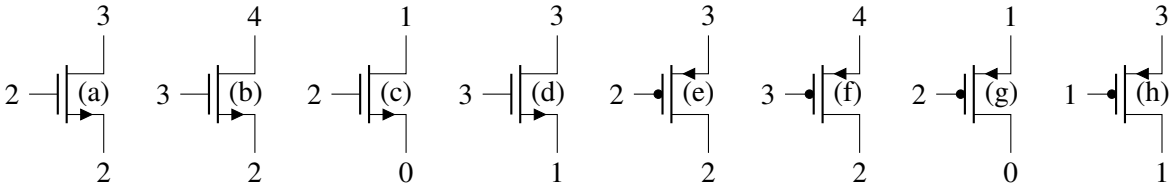
$$\Delta V_{GS} = (V_{GS} - V_t)\left(\sqrt{10} - 1\right) \approx 216\text{mV} \approx 200\text{mV}$$

Rubric: (2 Points)

- +1: Correct equation
- +1: Correct numerical value

6. (Fall 2009 Midterm 1 Q1)

For the following problems, the drain, gate, and source voltages are given. You may assume $V_{SB} = 0$V and that $V_{tn} = -V_{tp} = 0.5$V. Indicate if the devices are off, in the linear or triode region, or in saturation. If the devices are in saturation, calculate $|V_{dsat}|$.



	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)
Off/Lin/Sat								
V_{dsat} (if Sat)								

Solution:

	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)
Off/Lin/Sat	Off	Sat	Lin	Sat	Sat	Sat	Off	Sat
V_{dsat} (if Sat)		0.5		1.5	0.5	0.5		1.5

Rubric: (16 Points)

- +1: Each correct answer

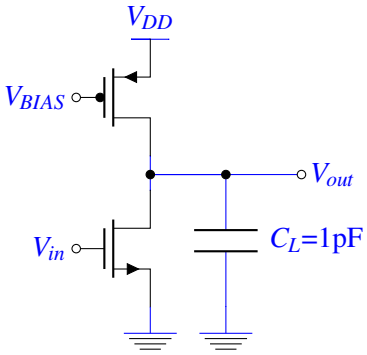
7. Common Source Amp Design

The parameters for a particular 0.5µm CMOS process are:

- $C_{ox} = 5\frac{\text{fF}}{\mu\text{m}^2}$
- $C_{ol} = 0.5\frac{\text{fF}}{\mu\text{m}}$
- $\mu_n C_{ox} = 2\mu_p C_{ox} = 200\frac{\mu\text{A}}{\text{V}^2}$
- $\lambda = \frac{1}{10\text{V}}$ when $L = 0.5\mu$m
- $V_{tn} = -V_{tp} = 0.5$V
- $V_{DD} = 2$V

(a) Design an NMOS-input common source amplifier with a PMOS load with a low frequency gain of approximately 200V/V, a unity gain frequency of 1Grad/s with a 1pF load, and an output swing of at least 300mV to 2.2V with a 2.5V single-sided supply. **Minimize power consumption.** Clearly indicate what values you are using for g_m, r_o, I_D, V_{dsat}, gate bias, W, and L for each transistor. Clearly indicate which parameters you "pick", and which you solve for. Calculate the input capacitance.

Solution:



This is a lot to take in! We'll deal with these by groupings of large(ish) signal vs. small signal:

Output swing: This puts a lower bound on the overdrive voltage we can have for our devices (that is, it can't exceed 300mV). $\longrightarrow V_{ovn}, V_{ovp} \leq 300\text{mV}$.

Looking at the small signal specifications we're trying to meet:

$$A_{v0} = g_m R_o \approx 200$$
$$\omega_u = \frac{g_m}{C_{\text{out}}} \approx 1\text{Grad/s}$$

Note that we used C_{out} rather than just C_L—if you have large devices, it could be that C_{out} is significantly larger than C_L. We could write down more equations, but it wouldn't really get us anywhere, so we need to choose a starting point.

The "I'm Taking The Exam and We Don't Get Calculators" Solution

The following is just an example of a design methodology which assumes you're taking an exam and don't have time to write code to actually check this super rigorously; you're by no means required to follow it exactly or even remotely closely.

i. Choose the output bias to be $V_{DD}/2$. This puts us almost-not-quite in velocity saturation, but for the sake of simplicity we'll assume we're in saturation $\longrightarrow \left(\frac{W}{L}\right)_p = 2\left(\frac{W}{L}\right)_n$, so $V_{ovp} = V_{ovn}$
ii. Another common starting point is choosing a V_{ov} of our devices. A standard "safe" overdrive voltage is around 200mV, and by safe we mean robust against process/temperature/etc. variation. $\longrightarrow V_{ov} = 200\text{mV}$
iii. Now we have a decent starting point, so consider the following equations:

$$g_m = \frac{2I_D}{V_{ov}}$$
$$R_o = \frac{r_o}{2} = \frac{1}{2\lambda I_D}$$
$$A_{v0} = \frac{1}{V_{ov}\lambda} \geq 200$$
$$\lambda \leq \frac{1}{200 \cdot 200\text{mV}}$$
$$= 0.025\text{V}^{-1}$$

and so we have to scale up our channel length to meet our gain requirement $\longrightarrow L = 2\mu\text{m}$

iv. At this point, all we have left to choose is W! Why is this? We've chosen our bias voltages, and I_D, g_m, and r_o are now fixed except for a linear (or inverse) relationship to W. To minimize power, we want to find the smallest W which still allows us to meet our small signal specification.
The equations that we'll use to verify everything:

$$I_D = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)V_{ov}^2(1+\lambda V_{DS})$$
$$\omega_u = \frac{g_m}{C_{\text{out}}}$$

This is where hand-iteration becomes more tenable, so we'll start by saying that $C_{out} = 1.1 \times C_L$ as a safe starting point. Then we can say that

$$g_m = \frac{\omega_u}{C_{\text{out}}}$$

to find the minimum W necessary to meet our specification. Then we go back and confirm that it actually works by explicitly finding C_{out}:

$$C_{\text{out}} \approx C_L + C_{gdp} + C_{dsp} + C_{dsn}$$

and iterate with the new C_{out} until we've converged on a W.

And then finally the equation for calculating input capacitance:

$$C_{in} \approx C_{gsn} + C_{gdn}(1 + g_m R_o)$$

The "We Have the Technology!" Solution

If you really want to minimize power, it's best to take advantage of the technology you have and make absolutely sure that you've exhausted all the possibilities for bias points. More specifically, rather than starting out by choosing an input/output bias, you would sweep both of them and test every single point to find one which meets your specification while consuming the smallest amount of I_D. The same goes for "choosing" V_{ov} of your devices; otherwise, the rest of the design methodology is largely the same.

Good Practice for the Real World

- Keep your devices the same channel length
- Make your devices integer multiples of a single width.

Side Note: When we perform all these calculations for gain, bandwidth, etc., we assume linear models for our devices. That is, we assume the input signal isn't large enough to effectively change the DC bias of our components; in reality, this often isn't true and is something that needs to be addressed more carefully (something you'll see in 240B!)

Rubric: (10 Points)

- +1: Correct equation for DC gain
- +1: Correct equation for ω_u
- +1: Correct lower bound for output swing
- +1: Correct upper bound for output swing

- +1: Correct equation for input capacitance (with reasonable approximation) including Millerized C_{gdn}
- +1: Correct equation for consumed power
- +4: Chose some starting point and from there made a reasonable effort at design

(b) How much could you change the input capacitance if you were primarily optimizing to minimize that?

Solution:

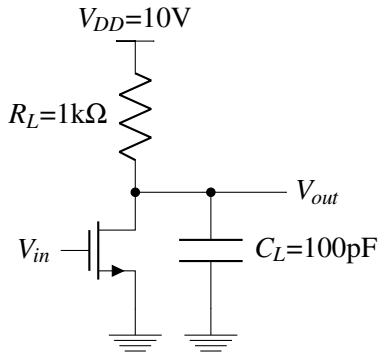
> In the example solution for minimizing power, we chose a starting point of bias voltages, calculated the necessary L, then and minimized W of our devices. Because our L is already fixed by our bias point, the strategy for minimizing power consumption above minimizes C_{in} for that particular bias point.
>
> If you wanted to be more aggressive, you could start by choosing (or sweeping) L first, then adjust your bias point to meet your gain and GBW spec (if it's even possible—sometimes it isn't!), and then finally minimize W.

Rubric: (5 Points)

- +2: Equation for input capacitance
- +3: Some reasonable explanation of how previous part's methodology could be altered to minimize C_{in}

8. Common Source With No Calculator

An NMOS common source amplifier has a 10V supply and a 1kΩ load (to the supply) in parallel with 100pF. Assume $\mu_n C_{ox} = 20\mu\text{A/V}^2$, $W/L = 10,000/1$, $V_{tn} = 1\text{V}$, and $\lambda = 0.01\text{V}$. You should be able to do all of the calculations by hand (without calculators). One-ish significant digits is fine.



(a) Write an expression for I_D as a function of output bias point. How much does I_D change as the output voltage varies from 9V to 1V?

Solution: First, we know

$$I_D = \frac{V_{DD} - V_{OUT}}{R_L}$$

Using this $V_{OUT} \in \{1, 9\}\text{V}$:

$$I_D(V_{OUT}=9\text{V}) = \frac{10-9}{10^3}\frac{\text{V}}{\Omega} = 1\text{mA}$$

$$I_D(V_{OUT}=1\text{V}) = \frac{10-1}{10^3}\frac{\text{V}}{\Omega} = 9\text{mA}$$

$$I_D = \frac{V_{DD}-V_{OUT}}{R_L}$$
$$I_D(V_{OUT}=9\text{V}) = 1\text{mA}$$
$$I_D(V_{OUT}=1\text{V}) = 9\text{mA}$$

Rubric: (3 Points)

- +1: Correct I_D equation
- +1: Correct I_D value (2×)

(b) What is the change in the input and overdrive voltage as the output varies from 9V to 1V?

Solution: Using the expression for overdrive voltage and our answer to the previous part to find the current,

$$V_{ov} = \sqrt{\frac{2I_D}{\mu C_{ox}\left(\frac{W}{L}\right)}}$$
$$V_{ov}(I_D = 1\text{mA}) = 0.1\text{V}$$
$$V_{ov}(I_D = 9\text{mA}) = 0.3\text{V}$$

$$@V_{OUT}=9\text{V} : V_{ov}=0.1\text{V}, V_{GS}=1.1\text{V}$$
$$@V_{OUT}=1\text{V} : V_{ov}=0.3\text{V}, V_{Gs}=1.3\text{V}$$

Rubric: (3 Points)

- +1: Correct V_{GS} equation
- +1: Correct V_{ov} value (2×)

(c) Write an expression for g_m and r_o as a function of output bias point.

Solution:

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)\left(\frac{V_{DD}-V_{OUT}}{R_L}\right)}$$
$$r_o = \frac{R_L}{\lambda(V_{DD}-V_{OUT})}$$

Rubric: (2 Points)

- +1: Correct g_m equation
- +1: Correct r_o equation

(d) Write an expression for a_{v0}—the intrinsic gain of the NMOS—as a function of output bias point.

Solution:

$$A_{v0} = \frac{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)\left(\frac{R_L}{V_{DD}-V_{OUT}}\right)}}{\lambda}$$

Rubric: (2 Points)

- +2: Correct intrinsic gain. If you approximated and derivated overall gain, that's fine too.

(e) Fill in the following table given the output bias point. Be sure to specify your units!

Output Bias Point	I_D	g_m	r_o	A_{v0}	ω_p	ω_u
9V						
6V						
1V						

Solution:

Output Bias Point	I_D	g_m	r_o	A_{v0}	ω_p	ω_u
9V	1mA	20mS	100kΩ	20	10Mrad/s	200Mrad/s
6V	4mA	40mS	25kΩ	40	10Mrad/s	400Mrad/s
1V	9mA	60mS	11.1kΩ	60	10Mrad/s	600Mrad/s

Rubric: (18 Points)

- +1: Correct g_m, r_o, a_{v0}, ω_p, and ω_u given the output bias value. $(5\times)$.
- Don't double-penalize—wrong I_D is -1, but the resulting r_o can still get credit if it was calculated correctly with the wrong I_D value.