EE 140/240A Linear Integrated Circuits
Fall 2019 Homework 5

This homework is due October 9, 2019, at 23:00.

Submission Format
Your homework submission should consist of **one** file.

- `hw5.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

1. MOSFET Small Signal Transconductances and Impedances

At low frequencies, single-transistor amplifiers' small signal model can be abstracted into the following form:

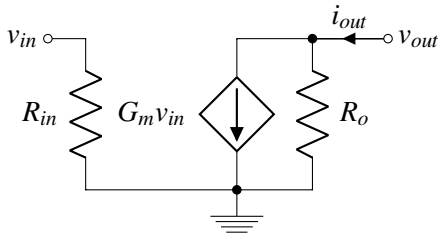


Figure 1: Generic amplifier

where, because our input does not depend in any way on our output (i.e. no feedback)

$$G_m = \frac{i_{out}}{v_{in}}|_{v_{out}=0\text{V}_{\text{AC}}} \qquad R_o = \frac{v_{out}}{i_{out}}|_{v_{in}=0\text{V}_{\text{AC}}}$$

$$\frac{v_{out}}{v_{in}} = -G_m R_o$$

It helps to have some things written out ahead of time (e.g. on your cheat sheet) to use as a reference. This might seem tedious, but you only have to do it once! **Your final answer should have both the full, unsimplified expression as as well a single simplified answer which uses the assumptions** $g_m r_o \gg 1$ **and** $R_D \approx R_S \approx r_o$

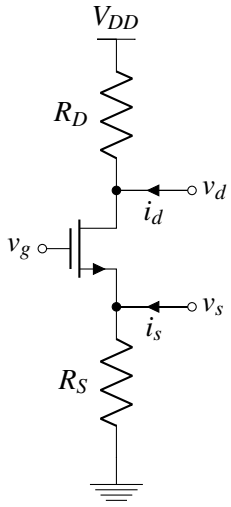


Figure 2: Various configurations of a single-transistor amplifier. Typical configurations are gate-to-drain, gate-to-source, and source-to-drain. Note that R_D and R_S can be replaced with complex impedances Z_D and Z_S, and your answers will still hold.

(a) $\frac{i_d}{v_g}$ given $v_d = 0\text{V}_{\text{AC}}$. This is the G_m of a degenerated common source.

(b) $\frac{v_d}{i_d}$ given $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a source-degenerated common source.

(c) $\frac{v_d}{v_g}$ assuming $R_D = \infty\Omega$. This is the voltage gain of a degenerated common source amplifier.

(d) $\frac{i_s}{v_g}$ given $v_s = 0\text{V}_{\text{AC}}$. This is the G_m of a source follower.

(e) $\frac{v_s}{i_s}$ given $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a source follower.

(f) $\frac{v_s}{v_g}$ assuming $R_S = \infty\Omega$. This is the voltage gain of a source follower.

(g) $\frac{i_d}{v_s}$ given $v_d = 0\text{V}_{\text{AC}}$ and $v_g = 0\text{V}_{\text{AC}}$. This is the G_m of a common gate amplifier.

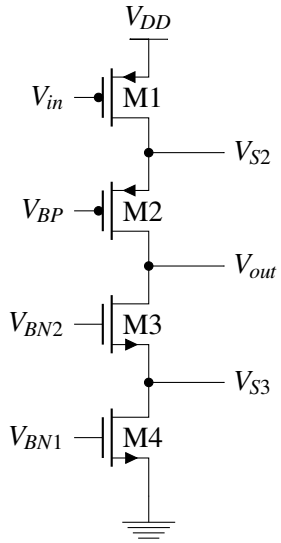
(h) $\frac{v_d}{i_d}$ given $v_s = 0\text{V}_{\text{AC}}$ and $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a common gate amplifier.

(i) $\frac{v_d}{v_s}$ given $v_g = 0\text{V}_{\text{AC}}$ and assuming $R_D = \infty\Omega$. This is the gain of a common gate amplifier.

(j) $\frac{v_s}{i_s}$ given $v_g = v_d = 0\text{V}_{\text{AC}}$ and $R_S = \infty\Omega$. This is the R_{in} of a common gate amplifier.

2. Cascode Analysis

For the circuit below, assume that $\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p$ and $\lambda_n = \lambda_p$ for all devices. You may assume that all devices are biased in saturation and that the quadratic model is appropriate. You may assume that $g_m r_o \gg 1$ for all combinations.



(a) Why must all devices have the same overdrive voltage?

(b) Assuming $V_{tn} = -V_{tp} = V_t$, what are the DC bias voltages on the gates of M1 and M4?

(c) What is the minimum voltage for the gate of M3 such that M4 stays in saturation? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

(d) What is the maximum voltage for the gate of M2 such that M1 stays in saturation? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

(e) If the gates of M2 and M3 are biased according to your answers above, what is the output swing (minimum to maximum voltage for both M2 and M3 to remain in saturation)? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

(f) What is the impedance seen "looking up" and "looking down" at the output, and the total impedance?

(g) What is the impedance looking up and down at the source of M3, and the total impedance?

(h) Is the total impedance seen at the source of M2 different from the source of M3? If not, why?

(i) What is the DC gain from the input to the output?

(j) What is the DC gain from the input to the source of M2?

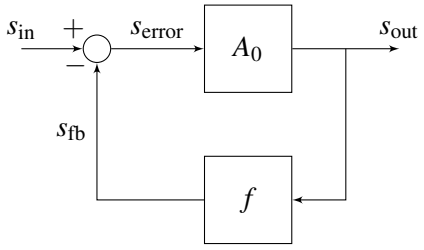
(k) What is the input capacitance? Express any device-specific capacitances (e.g. C_{gs}, C_{ds}, etc.) in terms of known quantities

(l) Given the total output capacitance of the amplifier is C_{out}, what are the pole and unity gain frequencies?

(m) If you double the overdrive voltages on all devices without changing the sizing of the devices, how does that affect the swing, DC gain, pole frequency, and unity gain frequency?

3. Gain Error

Given a feedback-only system, we usually approximate the closed loop gain $\frac{A_0}{1+A_0 f} \approx \frac{1}{f}$.



How good or bad an estimate is that? Show that the fractional gain error (gain error)/gain is $-\frac{1}{A_0 f}$

4. Gain Error in a Single-Pole Amplifier

In a single pole op-amp with $A_0 = 10^5 \text{V/V}$, $\omega_p = 1\text{krad/s}$, a feedback factor of $f = 0.01$ is used. Find:

(a) the exact low-frequency closed loop gain $\frac{A_0}{1+A_0 f}$. Use a calculator if necessary.

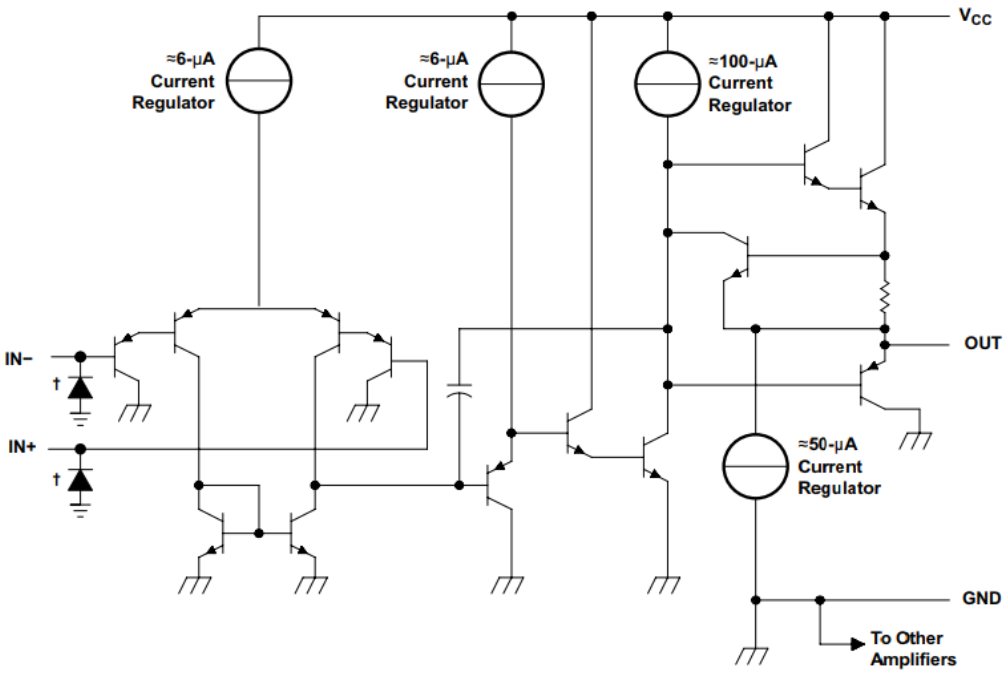
(b) the approximate low-frequency closed-loop gain, $\frac{1}{f}$.

(c) the fractional gain error $-\frac{1}{A_0 f}$. Does it agree with your results from parts (a) and (b)?

(d) Above the pole frequency, amplifier gain decreases and gain error increases. What is the fractional gain error at $10\omega_p$? $100\omega_p$?

5. LM324

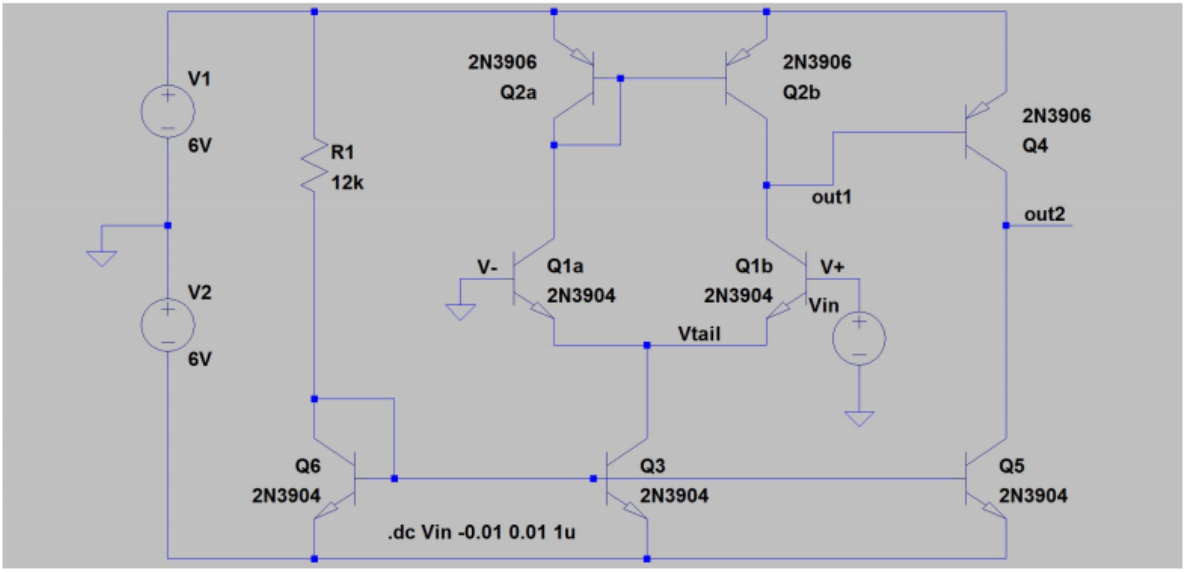
Check out the datasheet for the LM324 quad op-amp: http://www.ti.com/lit/ds/symlink/lm324.pdf.



(a) Circle and label the following in the diagram:

i. input differential pair (Darlington)
ii. current mirror active load
iii. emitter-follower level shifter(s)
iv. compensation capacitor
v. common emitter amplifier (Darlington)
vi. output stage

(b)



Assuming the same process parameters (e.g. V_A, β), how will the performance of the LM324 design compare to the amplifier above with a bias current of 1mA in the following areas

i. Input impedance. How does bias current and Darlington affect this?

ii. Impedance at the output of the first stage? How does the emitter-follower affect this?

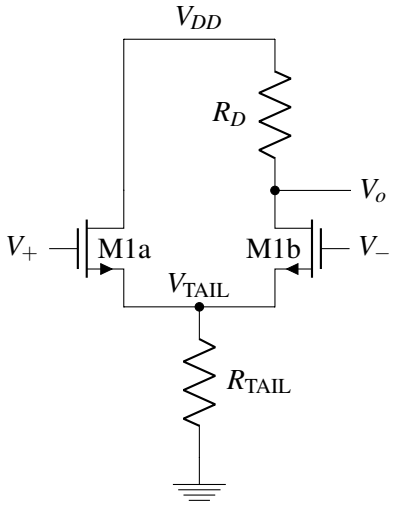
iii. Output impedance of the amplifier. How does output stage affect this?

(c) Given a diode-connected NPN transistor Q1 which has a 6µA reference current flowing through it, design a bipolar circuit to generate all four of the current supplies shown in the LM324 schematic. The 50µAand 100µA currents don't need to be exactly right, but should be close. Label your transistors as multiples of each other as appropriate, e.g. Q2 = 5Q1. You may assume infinite β.

(d) **(EE240A)** For the current supplies that you designed for the LM324 in part (c), estimate the actual current assuming a transistor β of 100. Use a beta helper to alleviate this problem. How much did the accuracy improve?

6. Differential Pair Drills

You may assume all transistors have $\lambda = 0$.



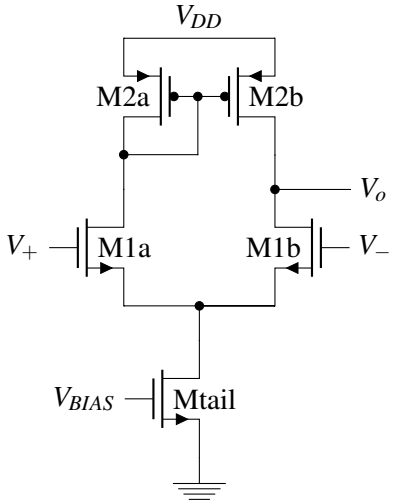
(a) For the circuit above, estimate the change in V_{TAIL}, I_{TAIL}, I_{D1a}, I_{D1b}, and V_o due to:
   i. An increase of ΔV in both V_+ and V_-
   ii. An increase of $\frac{\Delta V}{2}$ in V_+ and $-\frac{\Delta V}{2}$ in V_-
   iii. An increase of ΔV in just V_+

(b) What is the common mode rejection ratio of this amplifier?

(c) What is the common mode input range in terms of V_{tn} and V_{ov}?

(d) Sketch V_{ov} vs. V_{CM} over the input range from part (c)

(e) Sketch the bounds of the output swing over the input range from part (c)



(f) For the circuit above, estimate the change in V_{TAIL}, I_{TAIL}, I_{D1a}, I_{D1b}, and V_o due to an increase of ΔV in both V_+ and V_-. **Do not assume $\lambda = 0$.**

(g) What is the common mode input range in terms of V_{tn} and V_{ov}?

(h) Sketch V_{ov} vs. V_{CM} over the input range from part (g)

(i) Skech the bounds of the output swing over the input range from part (g)

7. Two-Stage Amplifier

(a) Design a 2-stage NMOS input CMOS op-amp with the following specs:

- 80µA tail current
- Able to sink 200µA from the load
- Output swing to within 200mV of the rails
- Input common mode range to within 200mV of the top rail
- Up to one resistor in the design

Your process technology has the following specs:

- $\mu_n C_{ox} = 2\mu_p C_{ox} = 200\frac{\mu A}{V^2}$
- $V_{tn} = -V_{tp} = 0.5V$
- $C_{ox} = 5\frac{fF}{\mu m^2}$
- $\lambda = \frac{1}{5V}$
- $L_{\min} = 0.5\mu m$
- $C_{ol} = 0.5\frac{fF}{\mu m}$

Draw the schematic and label the device sizes.

(b) For your amplifier in part (a):

i. Calculate and tabulate I_D, V_{ov}, g_m, r_o, C_{gs}, and C_{gd} for all devices
ii. Calculate the first and second stage gain, and the overall gain for both differential and common mode signals.
iii. Calculate the common mode input range, and the variation in tail current over that range.
iv. Calculate the gain across C_{gd1a}.
v. Calculate the output pole frequency with a 100fF load capacitance.
vi. Calculate the input capacitance of the second stage for frequencies below the output pole.
vii. Calculate the first stage output pole frequency, assuming that it is lower than the output pole.
viii. Calculate the input capacitance of the second stage above the second stage unity gain frequency.

(c) **(EE240A)** If the same amplifier were run at $V_{ov} = 0V$, how would that affect the gains and pole frequency?