EE 140/240A Linear Integrated Circuits
Fall 2019 Homework 5

This homework is due October 9, 2019, at 23:00.

Submission Format
Your homework submission should consist of **one** file.

- `hw5.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

1. MOSFET Small Signal Transconductances and Impedances

At low frequencies, single-transistor amplifiers' small signal model can be abstracted into the following form:

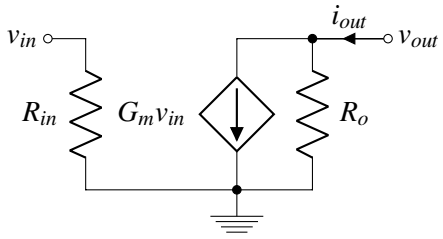


Figure 1: Generic amplifier

where, because our input does not depend in any way on our output (i.e. no feedback)

$$G_m = \frac{i_{out}}{v_{in}}|_{v_{out}=0\text{V}_{\text{AC}}} \qquad R_o = \frac{v_{out}}{i_{out}}|_{v_{in}=0\text{V}_{\text{AC}}}$$

$$\frac{v_{out}}{v_{in}} = -G_m R_o$$

It helps to have some things written out ahead of time (e.g. on your cheat sheet) to use as a reference. This might seem tedious, but you only have to do it once! **Your final answer should have both the full, unsimplified expression as as well a single simplified answer which uses the assumptions** $g_m r_o \gg 1$ **and** $R_D \approx R_S \approx r_o$

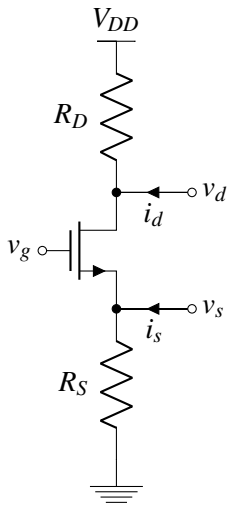


Figure 2: Various configurations of a single-transistor amplifier. Typical configurations are gate-to-drain, gate-to-source, and source-to-drain. Note that R_D and R_S can be replaced with complex impedances Z_D and Z_S, and your answers will still hold.

(a) $\frac{i_d}{v_g}$ given $v_d = 0\text{V}_{\text{AC}}$. This is the G_m of a degenerated common source.
Solution:

$$\frac{i_d}{v_g} = \frac{g_m r_o}{r_o + R_S + g_m r_o R_s}$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(b) $\frac{v_d}{i_d}$ given $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a source-degenerated common source.
Solution:

$$\frac{i_d}{v_d} = R_D || (r_o + R_S + g_m r_o R_S)$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(c) $\frac{v_d}{v_g}$ assuming $R_D = \infty\Omega$. This is the voltage gain of a degenerated common source amplifier.
Solution: Here you can use the answers from parts (a) and (b). For the latter, because R_D is infinite, $R_o = r_o + R_S + g_m r_o R_S$

$$\frac{v_d}{v_g} = -g_m r_o$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(d) $\frac{i_s}{v_g}$ given $v_s = 0\text{V}_{\text{AC}}$. This is the G_m of a source follower.

Solution:

$$\frac{i_s}{v_g} = -\frac{g_m r_o}{r_o + R_D}$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(e) $\frac{v_s}{i_s}$ given $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a source follower.

Solution:

$$\frac{i_s}{v_s} = R_S || \frac{r_o + R_D}{1 + g_m r_o}$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(f) $\frac{v_s}{v_g}$ assuming $R_S = \infty\Omega$. This is the voltage gain of a source follower.

Solution:

$$\frac{v_s}{v_g} = \frac{g_m r_o}{1 + g_m r_o}$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(g) $\frac{i_d}{v_s}$ given $v_d = 0\text{V}_{\text{AC}}$ and $v_g = 0\text{V}_{\text{AC}}$. This is the G_m of a common gate amplifier.

Solution:

$$\frac{i_d}{v_s} = -\frac{1 + g_m r_o}{r_o}$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(h) $\frac{v_d}{i_d}$ given $v_s = 0\text{V}_{\text{AC}}$ and $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a common gate amplifier.
Solution:

$$\frac{i_d}{v_d} = r_o || R_D$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(i) $\frac{v_d}{v_s}$ given $v_g = 0\text{V}_{\text{AC}}$ and assuming $R_D = \infty\Omega$. This is the gain of a common gate amplifier.
Solution:

$$\frac{v_d}{v_s} = 1 + g_m r_o$$

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

(j) $\frac{v_s}{i_s}$ given $v_g = v_d = 0\text{V}_{\text{AC}}$ and $R_S = \infty\Omega$. This is the R_{in} of a common gate amplifier.
Solution: Errata: The drain should not have been set to 0! Note that even in low frequencies, it's finite!

$$\frac{v_s}{i_s} = \frac{r_o}{1 + g_m r_o}$$

when $v_d = 0\text{V}_{\text{AC}}$, and

$$\frac{r_o + R_D}{1 + g_m r_o}$$

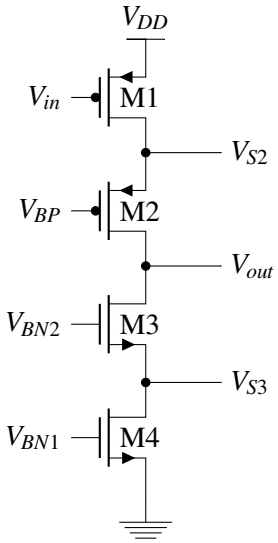
if you didn't tie it to 0.

Rubric: (2 Points)

- +1: Correct sign
- +1: Correct expression (without the sign)

2. Cascode Analysis

For the circuit below, assume that $\mu_n C_{ox} (W/L)_n = \mu_p C_{ox} (W/L)_p$ and $\lambda_n = \lambda_p$ for all devices. You may assume that all devices are biased in saturation and that the quadratic model is appropriate. You may assume that $g_m r_o \gg 1$ for all combinations.



(a) Why must all devices have the same overdrive voltage?

Solution:

All devices have the same current running through them, and their $\mu C_{ox}(W/L)$ and λ are all the same, so their overdrive voltages must all be the same as well.

Rubric: (1 Points)

- +1: Correct explanation

(b) Assuming $V_{tn} = -V_{tp} = V_t$, what are the DC bias voltages on the gates of M1 and M4?

Solution: First, we'll define $k \equiv \mu_{n/p} C_{ox} \left(\frac{W}{L}\right)_{n/p}$ for convenience.

$$V_{ov} = \sqrt{\frac{2I_D}{k}}$$

Because we know the source voltage of both of these devices, we can quickly find the gate bias with

$$V_{GSn/SGp} = V_t + V_{ov}$$

$$V_{G4} = V_{DD} - V_t - \sqrt{\frac{2I_D}{\mu C_{ox}\left(\frac{W}{L}\right)}}$$

$$V_{G1} = V_t + \sqrt{\frac{2I_D}{\mu C_{ox}\left(\frac{W}{L}\right)}}$$

Rubric: (2 Points)

- +1: Correct M1 gate bias. Full credit if you just used V_{ov} rather than the full expression with I_D, etc.

- +1: Correct M4 gate bias. Full credit if you just used V_{ov} rather than the full expression with I_D, etc.

(c) What is the minimum voltage for the gate of M3 such that M4 stays in saturation? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

Solution: To ensure M4 stays in saturation, $V_{DS4} \geq V_{ov}$. In other words, $V_{S3} \geq V_{ov}$

$$\begin{aligned} V_{DS4} &\geq V_{ov} \\ V_{S3} &\geq V_{ov} \\ -V_{GS3} + V_{G3} &\geq V_{ov} \\ -(V_t + V_{ov}) + V_{G3} &\geq V_{ov} \\ V_{G3} &\geq V_t + 2V_{ov} \end{aligned}$$

$$\boxed{V_{G3} \geq V_t + 2V_{ov}}$$

Rubric: (2 Points)

- +1: Correct minimum gate voltage

(d) What is the maximum voltage for the gate of M2 such that M1 stays in saturation? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

Solution: Following a similar process as (c)

$$\boxed{V_{G2} \leq V_{DD} - 2V_{ov} - V_t}$$

Rubric: (1 Points)

- +1: Correct M2 maximum gate voltage

(e) If the gates of M2 and M3 are biased according to your answers above, what is the output swing (minimum to maximum voltage for both M2 and M3 to remain in saturation)? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

Solution: With all the source voltages set appropriately, the output can swing down to $2V_{ov}$ or up to $V_{DD} - 2V_{ov}$

$$\boxed{V_{OUT} \in [2V_{ov}, V_{DD} - 2V_{ov}]}$$

Rubric: (2 Points)

- +1: Correct upper bound
- +1: Correct lower bound

(f) What is the impedance seen "looking up" and "looking down" at the output, and the total impedance?

Solution: From the previous parts, we know $g_m = \frac{2I_D}{V_{ov}}$ and $r_o = \frac{1}{\lambda I_D}$ as the same for all devices, but for completeness we'll include the full expression.

Looking up, we see:

$$\begin{aligned} R_{\text{out,up}} &= r_{o2} + g_{m2} r_{o2} r_{o1} + r_{o1} \\ &= g_m r_o^2 + 2r_o \end{aligned}$$

And looking down, the computation is identical:

$$\begin{aligned} R_{\text{out,down}} &= r_{o3} + g_{m3} r_{o3} r_{o4} + r_{o4} \\ &= g_m r_o^2 + 2r_o \end{aligned}$$

The total impedance is simply the parallel combination of the two

$$\begin{aligned} R_{\text{out}} &= R_{\text{out,up}} || R_{\text{out,down}} \\ &= \frac{g_m r_o^2 + 2r_o}{2} \end{aligned}$$

$$\begin{aligned} R_{\text{out,up}} &= R_{\text{out,down}} = g_m r_o^2 + 2r_o \\ R_{\text{out}} &= \tfrac{g_m r_o^2 + 2r_o}{2} \end{aligned}$$

Rubric: (3 Points)

- +1: Correct looking up impedance
- +1: Correct looking down impedance
- +1: Correct output impedance

(g) What is the impedance looking up and down at the source of M3, and the total impedance?

Solution: Looking up from the source of M3, we see:

$$\begin{aligned} R_{\text{S3,up}} &= \frac{r_{o3} + R_{\text{out,up}}}{1 + g_{m3} r_{o3}} \\ &= \frac{g_m r_o^2 + 3r_o}{1 + g_m r_o} \end{aligned}$$

And looking down, we simply see

$$\begin{aligned} R_{\text{S3,down}} &= r_{o4} \\ &= r_o \end{aligned}$$

Once again, the total impedance is the parallel combination of the two:

$$\begin{aligned} R_{\text{S3}} &= r_o || \frac{g_m r_o^2 + 3r_o}{1 + g_m r_o} \\ &= \left(\frac{1}{r_o} + \frac{1 + g_m r_o}{g_m r_o^2 + 3r_o} \right)^{-1} \\ &= \left(\frac{g_m r_o + 3 + 1 + g_m r_o}{g_m r_o^2 + 3r_o} \right)^{-1} \\ &= \frac{r_o (g_m r_o + 3)}{2 g_m r_o + 4} \end{aligned}$$

$$R_{S3,up} = \frac{g_m r_o^2 + 3r_o}{1 + g_m r_o}$$
$$R_{S3,down} = r_o$$
$$R_{S3} = \frac{r_o(g_m r_o + 3)}{2g_m r_o + 4}$$

Rubric: (3 Points)

- +1: Correct looking up impedance
- +1: Correct looking down impedance
- +1: Correct output impedance

(h) Is the total impedance seen at the source of M2 different from the source of M3? If not, why?

Solution:

The two impedances are the same! The same current flows through all devices which have the same $\mu C_{ox}\frac{W}{L}$.

(i) What is the DC gain from the input to the output?

Solution:

$$\begin{aligned} A_{v0} &= -G_m R_{out} \\ &= -g_{m1} R_{out} \\ &= -\frac{g_m^2 r_o^2 + 2g_m r_o}{2} \end{aligned}$$

$$A_{v0} = -\frac{g_m^2 r_o^2 + 2g_m r_o}{2}$$

Rubric: (1 Points)

- +1: Correct expression

(j) What is the DC gain from the input to the source of M2?

Solution:

$$\begin{aligned} \frac{v_{S2}}{v_{in}} &= -g_{m1} R_{S2} \\ &= -g_m R_{S2} \\ &= -\frac{g_m r_o (g_m r_o + 3)}{2g_m r_o + 4} \end{aligned}$$

$$A_{v0,S2} = -\frac{g_m r_o (g_m r_o + 3)}{2g_m r_o + 4}$$

Rubric: (1 Points)

- +1: Correct expression

(k) What is the input capacitance? Express any device-specific capacitances (e.g. C_{gs}, C_{ds}, etc.) in terms of known quantities

Solution: Notice that the Millerization term is only $A_{v0,S2}$, and not the full A_{v0}!

$$\begin{aligned} C_{\text{in}} &\approx C_{gs1} + (1 - A_{v0,S2} C_{gd1}) \\ &= C_{gs1} + (1 - A_{v0,S2}) C_{gd} \\ &= \left[\frac{2}{3} WLC_{ox} + WC_{ol}\right] + \left(1 + \frac{g_m r_o (g_m r_o + 3)}{2 g_m r_o + 4}\right) WC_{ol} \end{aligned}$$

$$C_{\text{in}} \approx \left[\frac{2}{3} WLC_{ox} + WC_{ol}\right] + \left(1 + \frac{g_m r_o (g_m r_o + 3)}{2 g_m r_o + 4}\right) WC_{ol}$$

Rubric: (2 Points)

- +1: Correct C_{in} equation
- +1: Correct value

(l) Given the total output capacitance of the amplifier is C_{out}, what are the pole and unity gain frequencies?

Solution: The unity gain frequency:

$$\omega_u = \frac{g_{m1}}{C_{\text{out}}}$$

The output pole:

$$\begin{aligned} \omega_p &= \frac{1}{R_{\text{out}} C_{\text{out}}} \\ &= \frac{2}{C_{\text{out}} (g_m r_o^2 + 2 r_o)} \end{aligned}$$

$$\omega_u = \frac{g_{m1}}{C_{\text{out}}}$$

$$\omega_p = \frac{2}{C_{\text{out}} (g_m r_o^2 + 2 r_o)}$$

Rubric: (3 Points)

- +1: Correct pole expression
- +1: Correct unity gain expression

(m) If you double the overdrive voltages on all devices without changing the sizing of the devices, how does that affect the swing, DC gain, pole frequency, and unity gain frequency?

Solution:

- *Swing*: Given the new overdrive $2V_{ov}$, the output swing is now limited to $[4V_{ov}, V_{DD} - 4V_{ov}]$
- *DC Gain*: $g_m = \frac{2I_D}{V_{ov}}$, so $g_m \uparrow 2\times$. $r_o = \frac{1}{\lambda I_D}$, so $r_o \downarrow 4\times$, meaning the overall $|A_{v0}| \downarrow 4\times$ (roughly)
- *Pole Frequency*: R_{out} decreases by roughly $8\times$, so C_{out} constant, $\omega_p \uparrow 8\times$

- *Unity Gain Frequency*: g_m doubles while C_{out} stays roughly constant, so ω_u doubles as well.

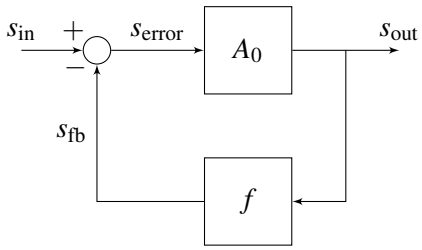
Swing	$[4V_{ov}, V_{DD} - 4V_{ov}]$
DC Gain	$\downarrow 4\times$
Pole Frequency	$\uparrow 8\times$
Unity Gain Frequency	$\uparrow 2\times$

Rubric: (4 Points)

- +1: Correct explanation for swing
- +1: Correct explanation for DC gain
- +1: Correct explanation for pole frequency
- +1: Correct explanation for unity gain frequency

3. Gain Error

Given a feedback-only system, we usually approximate the closed loop gain $\frac{A_0}{1+A_0 f} \approx \frac{1}{f}$.



How good or bad an estimate is that? Show that the fractional gain error (gain error)/gain is $-\frac{1}{A_0 f}$

Solution: Finding the gain error:

$$\begin{aligned}\frac{A_0}{1+A_0 f} - \frac{1}{f} &= \frac{A_0 f - 1 - A_0 f}{f(1+A_0 f)} \\ &= -\frac{1}{f(1+A_0 f)}\end{aligned}$$

And now the fraction of the ideal:

$$-\frac{1}{f(1+A_0 f)} \cdot f = -\frac{1}{1+A_0 f}$$

Consider a system in unity gain feedback with $A_0 = 1$—this means the fractional gain error is $-\frac{1}{2}$! That is, the output is half of what you estimated.

Fractional gain error: $-\frac{1}{1+A_0 f}$

This is only a good estimate when $A_0 f \gg 1$; when A_0 is low, this can lead to fairly significant systematic error!

Rubric: (5 Points)

- +2: Gain Error
- +2: Fraction of ideal
- +1: Comment on estimate

4. Gain Error in a Single-Pole Amplifier

In a single pole op-amp with $A_0 = 10^5 \text{V/V}$, $\omega_p = 1\text{krad/s}$, a feedback factor of $f = 0.01$ is used. Find:

(a) the exact low-frequency closed loop gain $\frac{A_0}{1+A_0 f}$. Use a calculator if necessary.
Solution:

$$\begin{aligned}\frac{A_0}{1+A_0 f} &= \frac{10^5}{1+10^5 \cdot 10^{-2}} \\ &= \frac{10^5}{1+10^3} \\ &\approx 99.9001\end{aligned}$$

$$A_{\text{closed-loop}} \approx 99.90 \frac{\text{V}}{\text{V}}$$

(b) the approximate low-frequency closed-loop gain, $\frac{1}{f}$.
Solution:

$$\frac{1}{f} = 100$$

(c) the fractional gain error $-\frac{1}{A_0 f}$. Does it agree with your results from parts (a) and (b)?
Solution:

$-\frac{1}{A_0 f} = -\frac{1}{1000}$ by definition agrees

(d) Above the pole frequency, amplifier gain decreases and gain error increases. What is the fractional gain error at $10\omega_p$? $100\omega_p$?
Solution: At $10\times$ and $100\times$ ω_p, the amplifier gain decreases by a factor of 10 and 100, respectively. As such, the fractional gain error $\left|-\frac{1}{A_0 f}\right|$ increases by a factor of 10 and 100 respectively from the DC error.

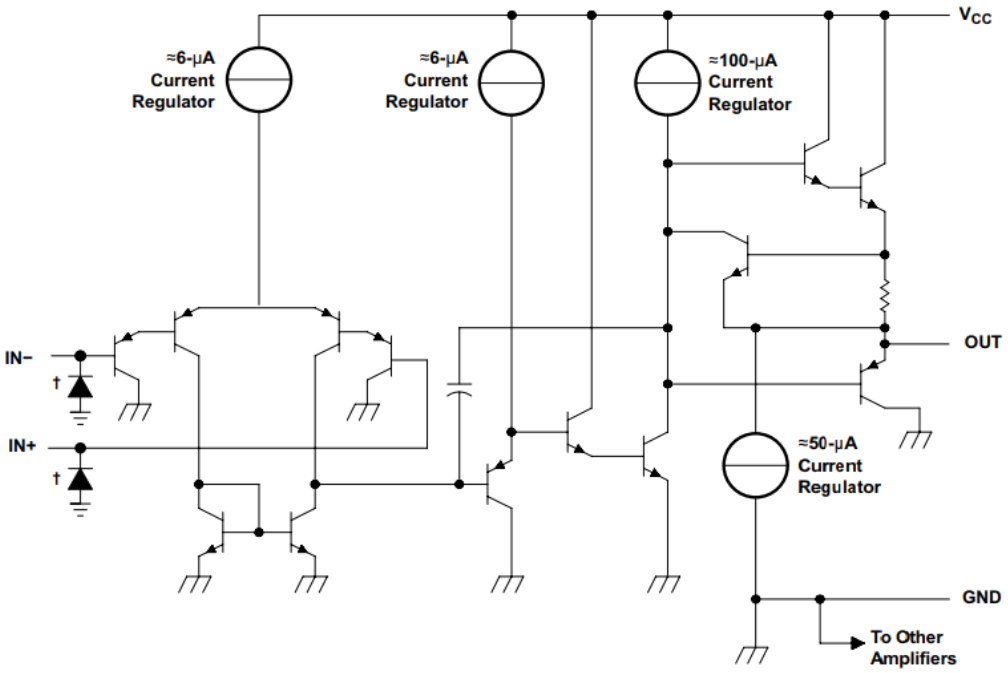
$$@10\text{MHz} : -\frac{1}{100}$$
$$@100\text{MHz} : -\frac{1}{10}$$

Rubric: (5 Points)

- +1 each for parts a-c.
- +2: For part d), 1 pt each for 10 and 100MHz

5. LM324

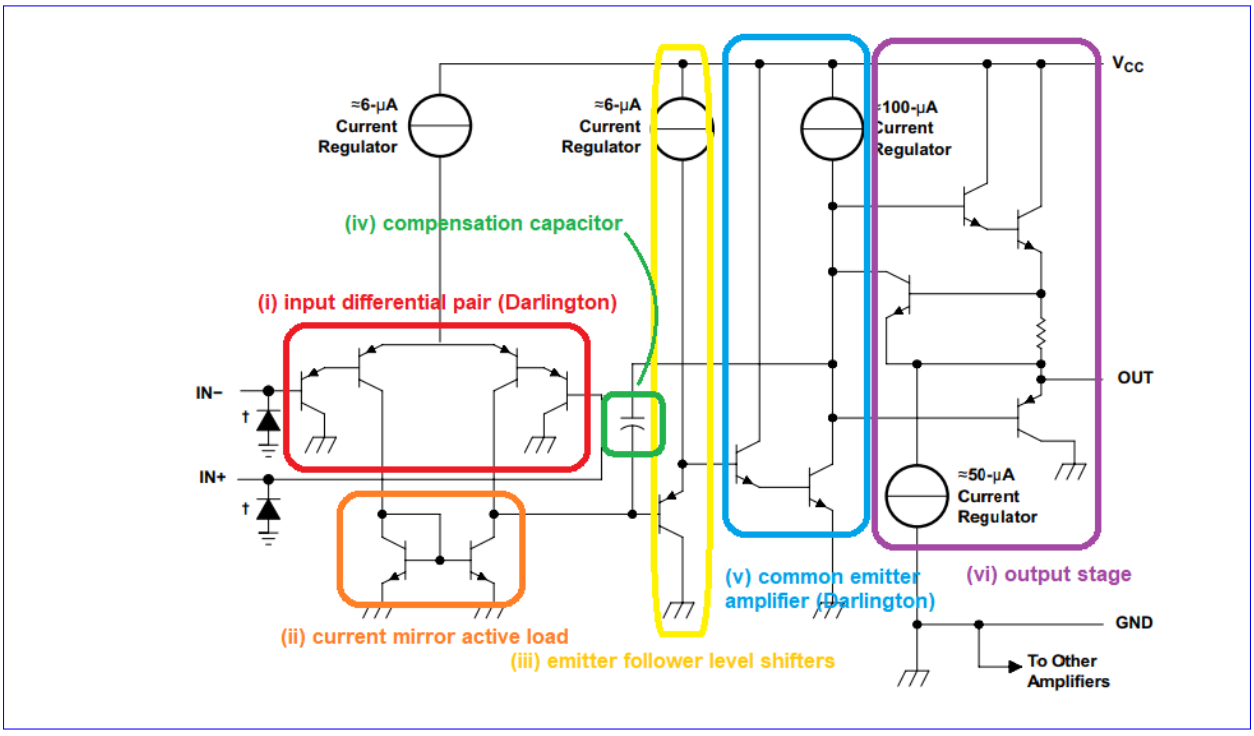
Check out the datasheet for the LM324 quad op-amp: http://www.ti.com/lit/ds/symlink/lm324.pdf.



(a) Circle and label the following in the diagram:

i. input differential pair (Darlington)
ii. current mirror active load
iii. emitter-follower level shifter(s)
iv. compensation capacitor
v. common emitter amplifier (Darlington)
vi. output stage

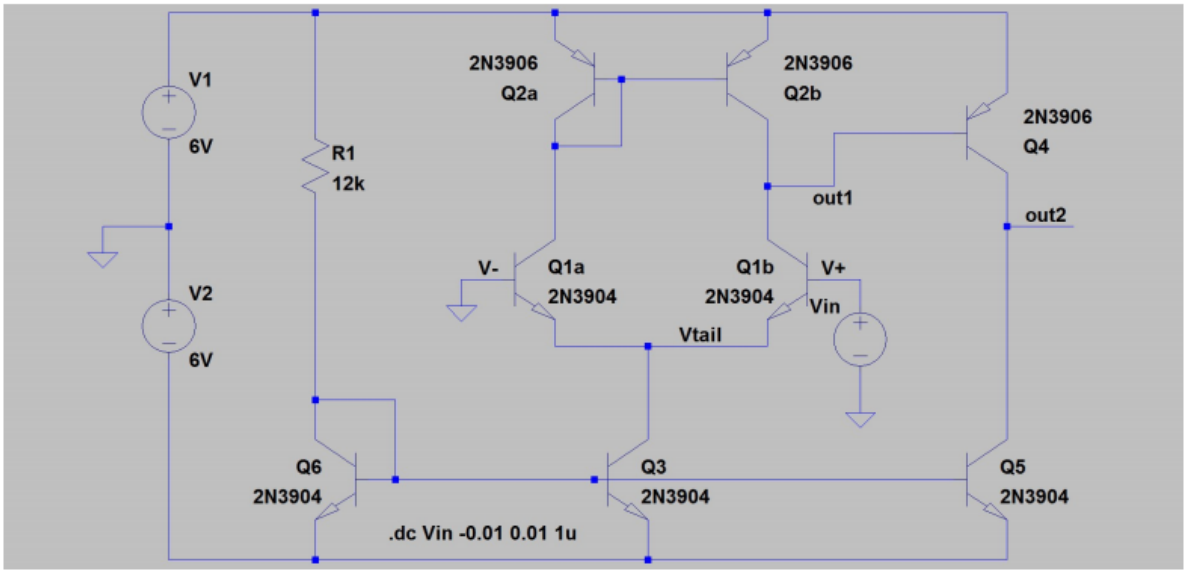
Solution:



Rubric: (6 Points)

- +1 Per correct label.

(b)



Assuming the same process parameters (e.g. V_A, β), how will the performance of the LM324 design compare to the amplifier above with a bias current of 1mA in the following areas

i. Input impedance. How does bias current and Darlington affect this?
Solution:

The LM324 has much higher input impedance. Not only is the bias current significantly lower (which reduces the input base current and increases input impedance), the input Darlington pair greatly reduces the base current as well, which further increases input impedance.

ii. Impedance at the output of the first stage? How does the emitter-follower affect this? **Rubric:** (6 Points)

- +2 per part, a-c.

Solution:

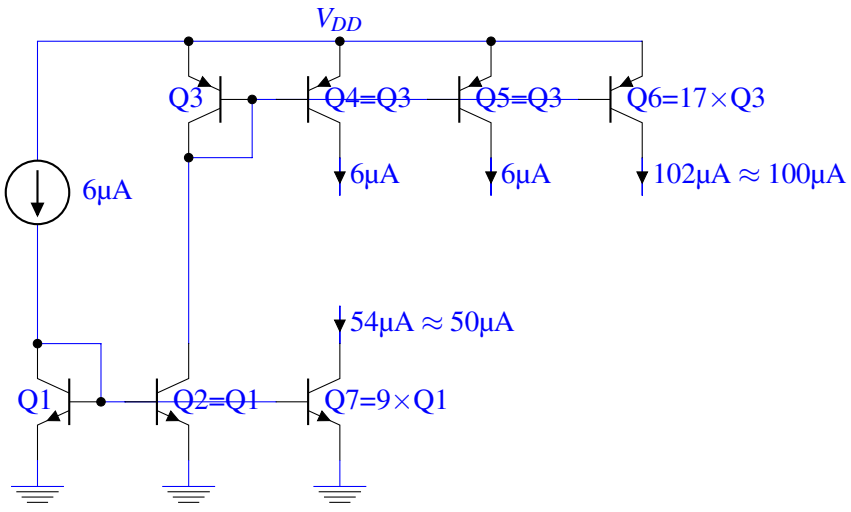
The common-emitter Darlington pair alleviates the loading effect of the second stage on the first. The level shifter provides an additional factor of β multiplying the impedance looking into the base of the Darlington pair.

iii. Output impedance of the amplifier. How does output stage affect this?
Solution:

The output impedance of the LM324 is given by teh output impedance of the Darlington pair, which is very small. In addition, the PMOS emitter follower has much lower output impedance.

(c) Given a diode-connected NPN transistor Q1 which has a 6µA reference current flowing through it, design a bipolar circuit to generate all four of the current supplies shown in the LM324 schematic. The 50µAand 100µA currents don't need to be exactly right, but should be close. Label your transistors as multiples of each other as appropriate, e.g. Q2 = 5Q1. You may assume infinite β.

Solution:



Rubric: (4 Points)

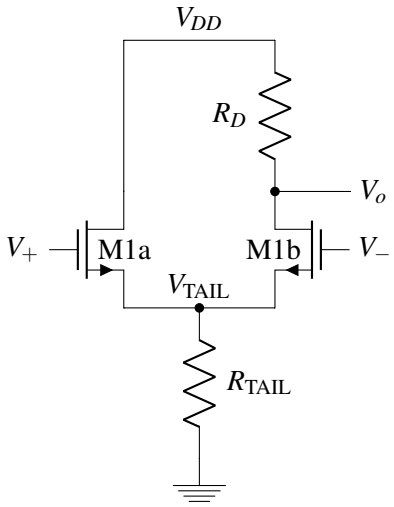
- +1 per correct sizing of 6, 50, and 100uA current sources (3 total).
- +1 for a working mirror schematic (npn vs pnp etc).

(d) **(EE240A)** For the current supplies that you designed for the LM324 in part (c), estimate the actual current assuming a transistor β of 100. Use a beta helper to alleviate this problem. How much did the accuracy improve? **Rubric:** (2 Points)

- +2 For effort.

6. Differential Pair Drills

You may assume all transistors have $\lambda = 0$.



(a) For the circuit above, estimate the change in V_{TAIL}, I_{TAIL}, I_{D1a}, I_{D1b}, and V_o due to:

i. An increase of ΔV in both V_+ and V_-

Solution: This is an increase in the common mode signal, so we consider the common mode characteristics of our amplifier (and in the process assume a linear model).

Because the gain from the inputs to V_{TAIL} is ≈ 1, V_{TAIL} increases by roughly ΔV.

$I_{\text{TAIL}} = \frac{V_{\text{TAIL}}}{R_{\text{TAIL}}}$, so I_{TAIL} increases by roughly $\frac{\Delta V}{R_{\text{TAIL}}}$.

$I_{D1a} \approx I_{D1b} \approx \frac{I_{\text{TAIL}}}{2}$, and so they increase by roughly $\frac{\Delta V}{2R_{\text{TAIL}}}$

$V_o = V_{DD} - I_{D1b}R_D$, so V_o moves by $-\Delta V \frac{R_D}{2R_{\text{TAIL}}}$

V_{TAIL}	$+\Delta V$
I_{TAIL}	$+\frac{\Delta V}{R_{\text{TAIL}}}$
I_{D1a}	$+\frac{\Delta V}{2R_{\text{TAIL}}}$
I_{D1b}	$+\frac{\Delta V}{2R_{\text{TAIL}}}$
V_o	$-\Delta V \frac{R_D}{2R_{\text{TAIL}}}$

Rubric: (5 Points)

- +1 Per correct item.

ii. An increase of $\frac{\Delta V}{2}$ in V_+ and $-\frac{\Delta V}{2}$ in V_-

Solution: This is functionally introducing a differential signal to the amplifier.

Because the g_m of the two devices is the same, there's no net change in current, meaning V_{TAILL} and I_{TAIL} don't change.

However, I_{D1a} will increase by $\frac{\Delta V}{2} g_{m1a}$, and I_{D1b} will change by $-\frac{\Delta V}{2} g_{m1b}$.
That said, $V_o = V_{DD} - I_{D1b} R_D$ will increase by $\frac{\Delta V}{2} g_m R_D$.

V_{TAIL}	No change
I_{TAIL}	No change
I_{D1a}	$+\frac{\Delta V}{2} g_{m1a}$
I_{D1b}	$-\frac{\Delta V}{2} g_{m1b}$
V_o	$+\frac{\Delta V}{2} g_{m1b} R_D$

Rubric: (5 Points)

- +1 Per correct item.

iii. An increase of ΔV in just V_+

Solution: This is essentially the same as introducing a DC bias of $+\frac{\Delta V}{2}$ on top of a differential signal, so we can use our answers to parts (a)i. and (a)ii..

V_{TAIL} will shift by $+\frac{\Delta V}{2}$ due to the common mode shift, and the differential signal will not affect it.

I_{TAIL} will shift by $+\frac{\Delta V}{2R_{\text{TAIL}}}$ due to the common mode shift, and the differential signal will not affect it.

Between the left and right branches, the change in I_{TAIL} will be split evenly for $+\frac{\Delta V}{4R_{\text{TAIL}}}$ for both I_{D1a} and I_{D1b}.

Purely from the differential signal, however, I_{D1a} will increase by $+g_{m1a}\frac{\Delta V}{2}$ and I_{D1b} will shift by $-g_{m1b}\frac{\Delta V}{2}$.
Finally, V_o will shift by the change in $-I_{D1b} R_D$.

V_{TAIL}	$+\frac{\Delta V}{2}$
I_{TAIL}	$+\frac{\Delta V}{2R_{\text{TAIL}}}$
I_{D1a}	$+\frac{\Delta V}{4R_{\text{TAIL}}} + g_{m1a}\frac{\Delta V}{2}$
I_{D1b}	$+\frac{\Delta V}{4R_{\text{TAIL}}} - g_{m1b}\frac{\Delta V}{2}$
V_o	$-R_D\left(+\frac{\Delta V}{4R_{\text{TAIL}}} - g_{m1b}\frac{\Delta V}{2}\right)$

Rubric: (5 Points)

- +1 Per correct item.

(b) What is the common mode rejection ratio of this amplifier?

Solution: Using our answers from parts (a)i. and (a)ii.,

$$\begin{aligned}\text{CMRR} &= \frac{A_{\text{diff}}}{A_{\text{CM}}} \\ &= \frac{g_{m1b}R_D}{2} \cdot \frac{2R_{\text{TAIL}}}{R_D} \\ &= g_{m1b}R_{\text{TAIL}}\end{aligned}$$

$$\boxed{\text{CMRR} = g_{m1b}R_{\text{TAIL}}}$$

Rubric: (2 Points)

- +1 Correct definition of CMRR.
- +1 Correct algebra.

(c) What is the common mode input range in terms of V_{tn} and V_{ov}?

Solution: We know the input has to be at least one threshold voltage above V_{TAIL} in order for the devices to be turned on, and if you're given an overdrive V_{ov} we know the gate voltage has to be another overdrive above the threshold addition:

$$\begin{aligned}V_{\text{G,min}} &= 2I_{D1b}R_{\text{TAIL}} + V_{tn} + V_{ov} \\ &= \frac{V_{\text{in,CM}} - V_{ov} - V_{tn}}{R_{\text{TAIL}}} \cdot R_{\text{TAIL}} + V_{tn} + V_{ov} \\ &= V_{ov} + V_{tn}\end{aligned}$$

On the upper bound, it's important to note that V_{TAIL} will track the input common mode as a source follower! on the other hand, as the input common mode increases, V_o decreases by a factor of $v_{\text{tail}}\frac{R_D}{2R_{\text{TAIL}}}$ (this refers to the small signal change in V_{tail}, not the actual DC bias).

This continues until $V_o - V_{\text{TAIL}} = V_{ov}$, after which point one of the devices will fall out of saturation.

We start by finding how high V_{TAIL} can get

$$\begin{aligned}V_{DD} &= V_{\text{TAIL}} + V_{ov} + I_{D1b}R_D \\ &= V_{\text{TAIL}} + V_{ov} + R_D\left(\frac{V_{\text{TAIL}}}{2R_{\text{TAIL}}}\right) \\ V_{\text{TAIL}}\left(1 + \frac{R_D}{2R_{\text{TAIL}}}\right) &= V_{DD} - V_{ov} \\ V_{\text{TAIL,max}} &= \frac{2R_{\text{TAIL}}(V_{DD} - V_{ov})}{2R_{\text{TAIL}} + R_D}\end{aligned}$$

and from here we know V_G can be V_{tn} greater than V_D, so

$$\begin{aligned}V_{\text{G,max}} &= V_{\text{TAIL,max}} + V_{ov} + V_{tn} \\ &= \frac{2(V_{DD} - V_{ov})R_{\text{TAIL}}}{R_D + 2R_{\text{TAIL}}} + V_{ov} + V_{tn}\end{aligned}$$

$$V_{\text{in,CM}} \in [V_{ov} + V_{tn}, \frac{2(V_{DD} - V_{ov})R_{\text{TAIL}}}{R_D + 2R_{\text{TAIL}}} + V_{ov} + V_{tn}]$$

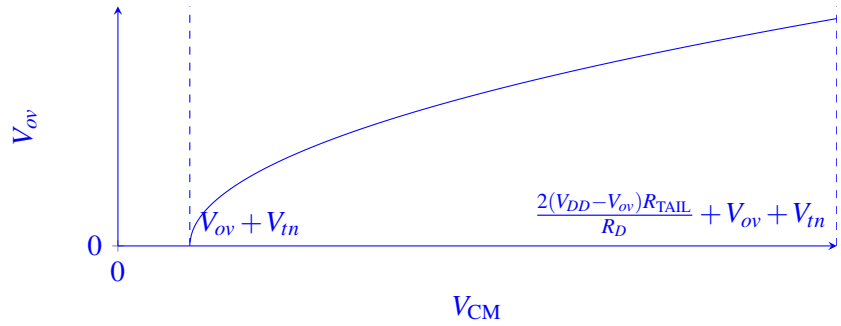
Rubric: (4 Points)

- +2 For correct upper bound.
- +2 For correct lower bound.

(d) Sketch V_{ov} vs. V_{CM} over the input range from part (c)

Solution:

$$V_{ov} \propto \sqrt{V_{\text{CM}}}$$

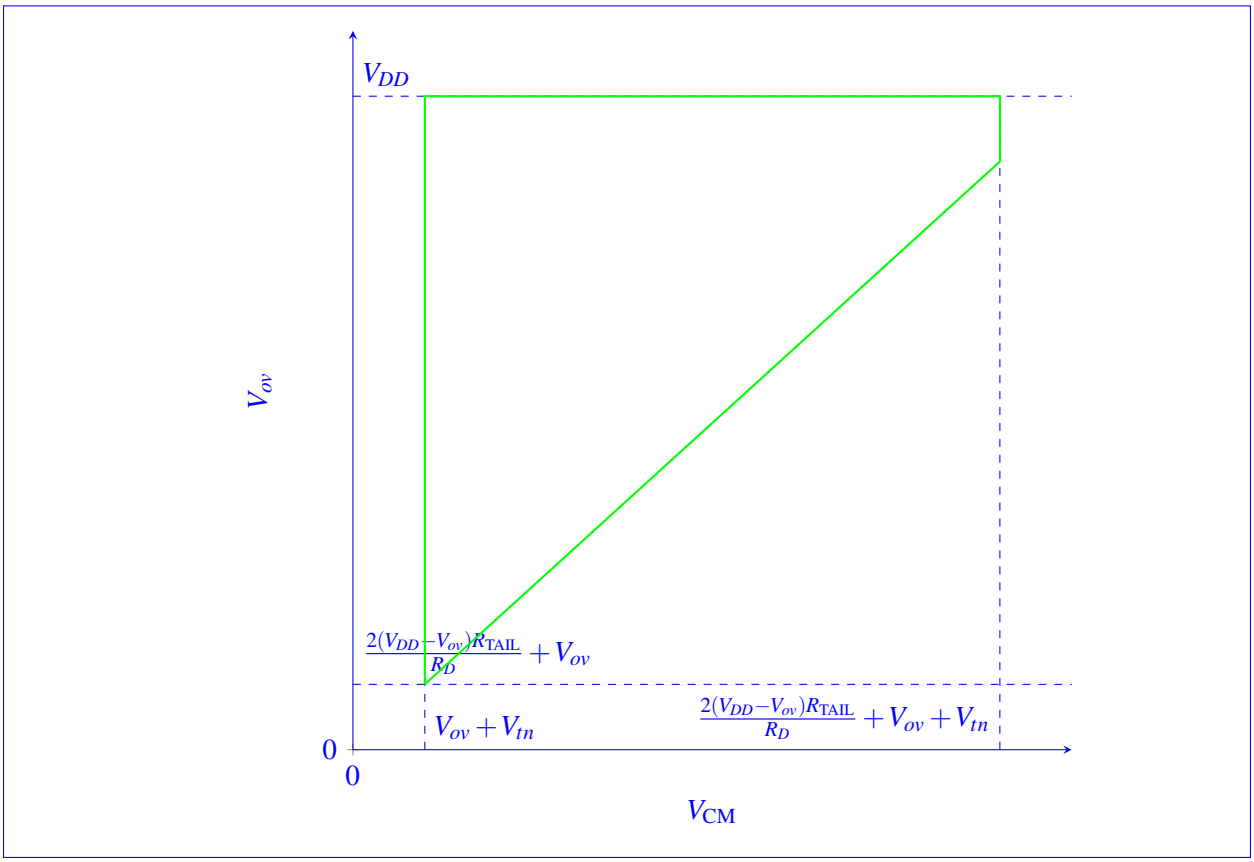


Rubric: (2 Points)

- +1 For correct proportionality.
- +1 For correct plot.

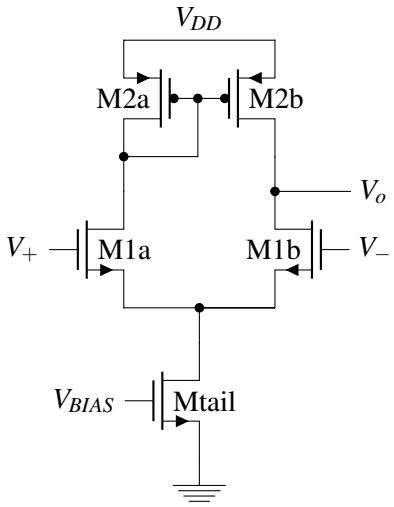
(e) Sketch the bounds of the output swing over the input range from part (c)

Solution:



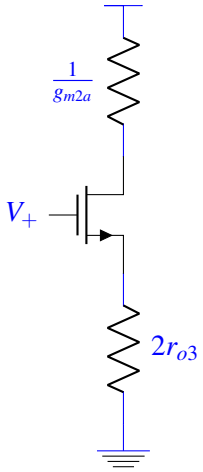
The outline has been marked in green for greater visibility. **Rubric:** (4 Points)

- +2 For correct region of output swing.
- +2 For rest of the plot.



(f) For the circuit above, estimate the change in V_{TAIL}, I_{TAIL}, I_{D1a}, I_{D1b}, and V_o due to an increase of ΔV in both V_+ and V_-. **Do not assume $\lambda = 0$.**

Solution: It helps to consider the (sort of) equivalent half circuit:



Once again, V_{TAIL} roughly tracks the input, so it shifts by $+\Delta V$.

Looking to the half circuit, I_{TAIL} changes by $+\frac{\Delta V}{r_{o3}}$ (mind your factors of 2!)

I_{D1a} and I_{D1b} change together by half the change in the tail current, $+\frac{\Delta V}{2r_{o3}}$.

And lastly, we know the common mode gain $A_{\text{CM}} = \frac{1}{2r_o g_{m2}}$, so V_o changes by $-\frac{\Delta V}{2r_o g_{m2}}$

V_{TAIL}	$+\Delta V$
I_{TAIL}	$+\frac{\Delta V}{r_{o3}}$
I_{D1a}	$+\frac{\Delta V}{2r_{o3}}$
I_{D1b}	$+\frac{\Delta V}{2r_{o3}}$
V_o	$-\frac{\Delta V}{2r_o g_{m2}}$

Rubric: (5 Points)

- +1 Per correct item.

(g) What is the common mode input range in terms of V_{tn} and V_{ov}?

Solution: On the low side,

$$V_{\text{CM,min}} = V_{ov3} + V_{ov1} + V_{tn}$$

And on the high side (going down the left branch):

$$V_{\text{CM,max}} = V_{DD} - (V_{ov2} + |V_{tp}| - V_{tn})$$

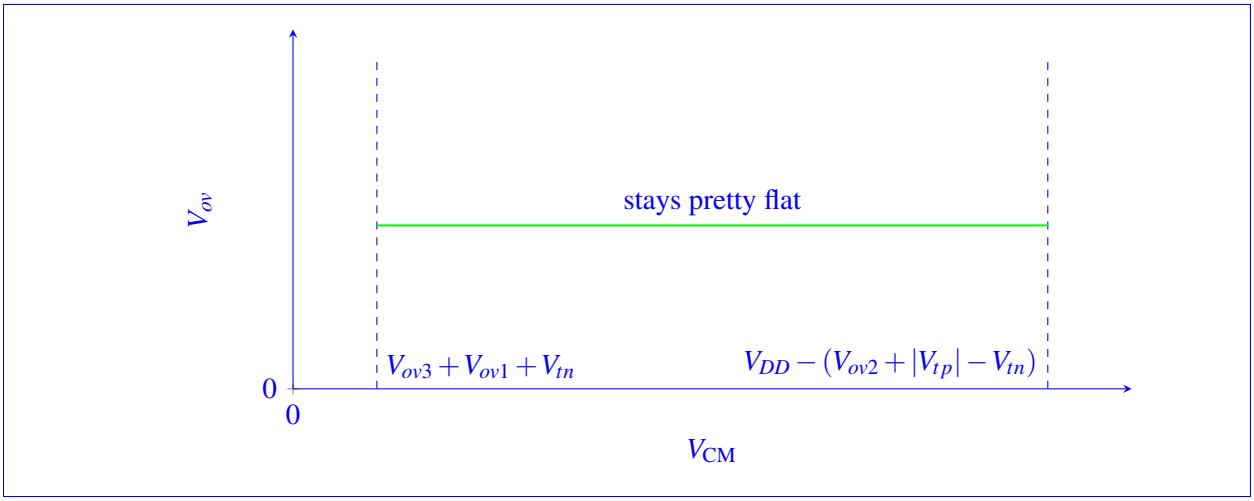
$$V_{\text{CM}} \in [V_{ov3} + V_{ov1} + V_{tn}, V_{DD} - (V_{ov2} + |V_{tp}| - V_{tn})]$$

Rubric: (4 Points)

- +2 Correct Low side.
- +2 Correct High Side.

(h) Sketch V_{ov} vs. V_{CM} over the input range from part (g)

Solution:

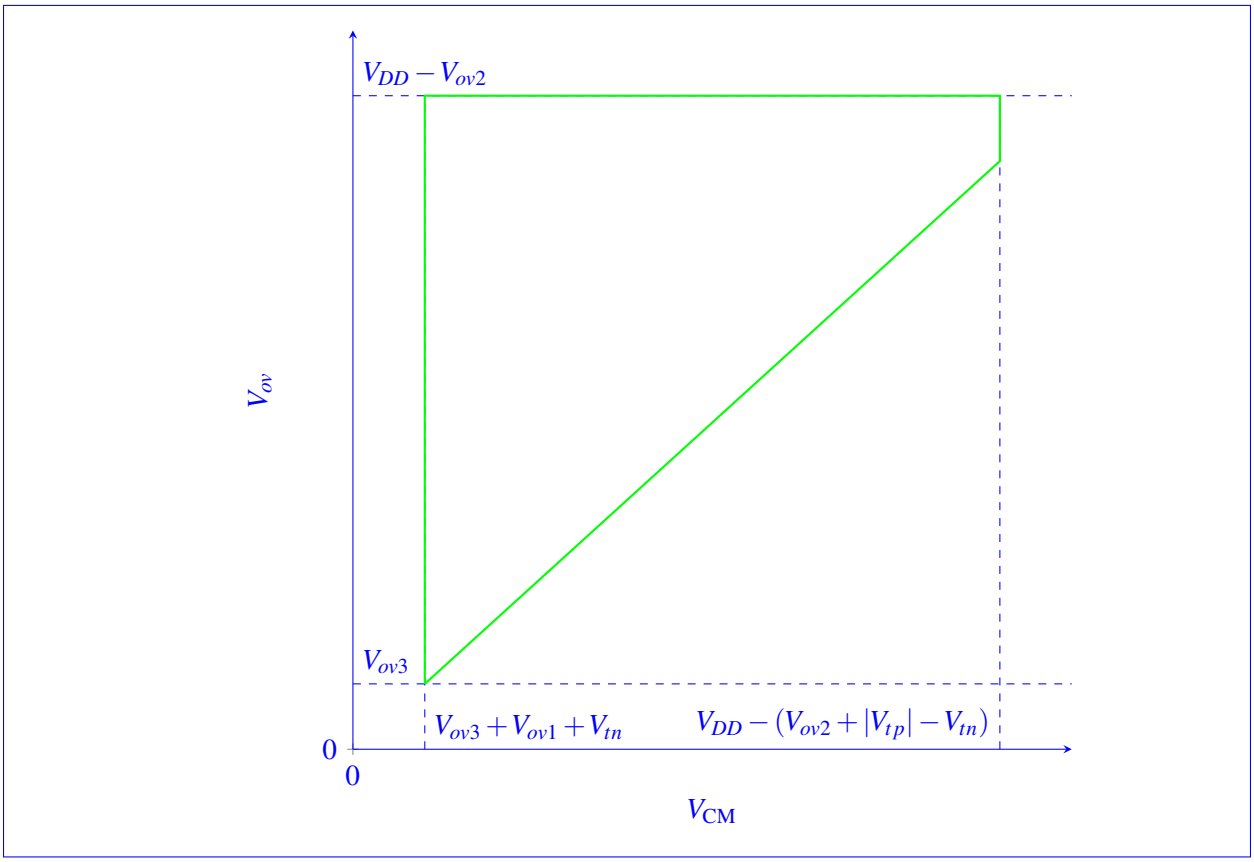


Rubric: (2 Points)

- +2 correct plot.

(i) Skech the bounds of the output swing over the input range from part (g)

Solution:



Rubric: (4 Points)

- +2 For correct region of output swing.
- +2 For rest of the plot.

7. Two-Stage Amplifier

(a) Design a 2-stage NMOS input CMOS op-amp with the following specs:

- 80µA tail current
- Able to sink 200µA from the load
- Output swing to within 200mV of the rails
- Input common mode range to within 200mV of the top rail
- Up to one resistor in the design

Your process technology has the following specs:

- $\mu_n C_{ox} = 2\mu_p C_{ox} = 200\frac{\mu A}{V^2}$
- $\lambda = \frac{1}{5V}$
- $V_{tn} = -V_{tp} = 0.5V$
- $L_{\min} = 0.5\mu m$
- $C_{ox} = 5\frac{fF}{\mu m^2}$
- $C_{ol} = 0.5\frac{fF}{\mu m}$
- $V_{DD} = 2V$

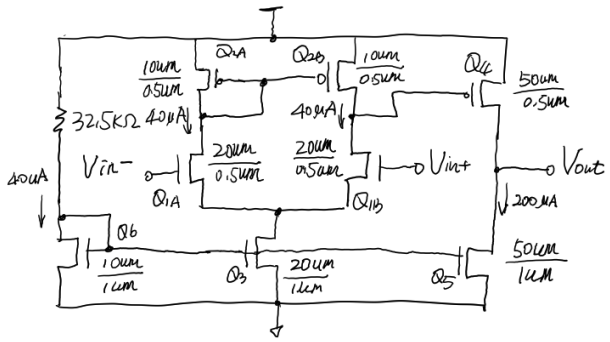
Draw the schematic and label the device sizes.

Solution: [20 pts] 1 for each W and L of the 8 transistors, 1 for labeling each of the for current. There aren't many things that you get to pick in this problem. You can pick L5, and then L3 and L6 should be the same. You can pick L2A, and then L2B and L4 should be the same. You can pick L1A, and then L1B should be the same. (W/L) for M3, M4, and M5 are all fixed by the specs. You have some flexibility in the overdrive voltage for M1, but Vov2 must be the same as Vov4 (which is set by spec) to get the right bias.

Some things to remember: $(W/L)_{1a} + (W/L)_{1b} = (W/L)_3$ if their overdrives are the same. $(W/L)_4 = (W/L)_5(\mu_n C_{ox})/(\mu_p C_{ox})$ if their overdrives are the same. $(W/L)_{2a} + (W/L)_{2b} = (W/L)_4(ID_3/ID_5)$.

From design specs, $I_{D3} = 80\mu A$, $I_{D4} = I_{D5} = 200\mu A$ (You can leave some margin here for $I_{D4} and I_{D5}$).
$|V_{ov4}| = V_{ov5} = 200mV$
$V_{ov3} = V_{ov5} = V_{ov6} = 200mV$ (You can also leave some margin for Vov's)
For input common-mode voltage, max value is
$V_{cm,max} = V_{DD} - V_{tp} - |V_{ov2}| + V_{tn} = V_{DD} - 200mV$
so, $V_{ov2} = 200mV$
To increase gm of input pair, we choose $V_{ov1} = 100mV$ (You can choose other values)

Then, we can calculate the size of all transistors (we choose $L = 1\mu m$ for current mirrors, for a larger output impedance and minimum length for other transistors).
$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 V_{ov}^2 = 80\mu A$
so, $\left(\frac{W}{L}\right)_3 = \frac{20um}{1um}$. Similarly,
$\left(\frac{W}{L}\right)_5 = \frac{50um}{1um}$ $\left(\frac{W}{L}\right)_4 = \frac{50um}{0.5um}$ $\left(\frac{W}{L}\right)_2 = \frac{10um}{0.5um}$ $\left(\frac{W}{L}\right)_1 = \frac{20um}{0.5um}$
We choose reference branch being $40\mu A$,
$\left(\frac{W}{L}\right)_6 = \frac{10um}{1um}$
And resistor is R,
$R = \frac{V_{DD} - V_{ov6} - V_{tn}}{I_{ref}} = 32.5K\Omega$
The device sizes are



(b) [35pts] For your amplifier in part (a):

i. Calculate and tabulate I_D, V_{ov}, g_m, r_o, C_{gs}, and C_{gd} for all devices
Solution: [18pts âĂŞ 1âĄĎ2 pt for each entry in the table above]
Note: Your size in previous question will affect all the following answers. So you might get different results depending on the size you use.

	Q1	Q2	Q3	Q4	Q5	Q6
I_D(A)	40μ	40μ	80μ	200μ	200μ	40μ
V_{ov}(V)	100m	200m	200m	200m	200m	200m
$g_m = \frac{2I_D}{V_{ov}}$(S)	0.8m	0.4m	0.8m	2m	2m	0.4m
$r_o = \frac{1}{\lambda I_D}(\Omega)$	125K	125K	125K	25K	50K	250K
$C_{gs} = \frac{2}{3}WLC_{ox} + WC_{ol}$(F)	43f	22f	77f	108f	192f	38f
$C_{gd} = WC_{ol}$(F)	10f	5f	10f	25f	25f	5f

ii. Calculate the first and second stage gain, and the overall gain for both differential and common mode signals.
Solution: [5 pts. 2 each for 1st and 2nd, 1 for overall]
$A_{v1,diff} = -g_{m1}(r_{o1}||r_{o2}) = -50$
$A_{v2,diff} = -g_{m4}(r_{o4}||r_{o5}) = -34$
$A_{v,diff} = A_{v1,diff}A_{v2,diff} = 1700$
$A_{v1,cm} = -\frac{2g_{m1}}{1+2g_{m1}r_{o3}}\frac{1}{2g_{m2}} = -0.01$
$A_{v,cm} = A_{v1,cm}A_{v2,diff} = 0.34$

iii. Calculate the common mode input range, and the variation in tail current over that range.
Solution: [2 pts]
$V_{cm,max} = V_{DD} - V_{ov2} - |V_{tp}| + V_{tn} = 1.8V$
$V_{cm,min} = V_{ov3} + V_{ov1} + V_{tn} = 0.8V$
$\Delta I_{DS3} = I_{D3}\lambda\Delta V_{DS3} = 80\mu\frac{1}{10}\cdot 1 = 8\mu A$

iv. Calculate the gain across C_{gd1a}.
Solution: [2 pts]
This question is not meant to be a tough problem, but it is if you want to do it right.
The simplest answer is $-\frac{g_{m1a}}{g_{m2a}} = -2$.
A better answer would take into account the source degeneration effect on Vtail, and come up with $-\frac{g_{m1a}}{1+g_{m1a}/g_{m1b}}gm_2a = -1$.
The best answer would be $R_{tail} = \frac{r_{o1}||r_{o2}+r_{o1}}{1+g_{m1}r_{o1}}||r_{o3} \approx \frac{3}{2g_{m1b}}$, and $Av = -\frac{g_{m1a}}{1+g_{m1a}R_{tail}}g_{m2a} = -4/5$
Any of those answers is fine. Bottom line: there is not much gain across that node, so not much Millerized input capacitance.

v. Calculate the output pole frequency with a 100fF load capacitance.

Solution: [2 pts]
$R_{out} = r_{o4}||r_{o5} = 17K\Omega$
$C_{out} \approx C_l + C_{gd4} + C_{gd5} = 150fF$
$\omega_{p,out} = \frac{1}{R_{out}C_{out}} = 392Mrad/s$

vi. Calculate the input capacitance of the second stage for frequencies below the output pole.
Solution: [2 pts]
$A_{v2} = g_{m4}r_{o4} = -34$
With Miller effect, $C_{in2} = C_{gd4}(1 - A_{v2}) + C_{gs4} = 983fF$

vii. Calculate the first stage output pole frequency, assuming that it is lower than the output pole.
Solution: [2 pts]
$R_{out1} = r_{o1}||r_{o2} = 62.5K\Omega$
$C_{out1} = C_{in2} + C_{gd1} + C_{gd2} = 998fF$
$\omega_{p,out1} = \frac{1}{R_{out1}C_{out1}} = 16Mrad/s$

viii. Calculate the input capacitance of the second stage above the second stage unity gain frequency.
Solution: [2 pts]
Above second stage unity gain frequency, there's neglectabe Miller effect, as gain becoming too small.
$C_{in2} = C_{gd4} + C_{gs4} = 133fF$

(c) **(EE240A)** If the same amplifier were run at $V_{ov} = 0$V, how would that affect the gains and pole frequency?

Solution: [10 pts]

When V_{ov} drops, transistor gm will increase. With same current, the gain will also increase. This trend will go on even when the transistor goes to subthreshold region. We also say that the effeciency of the transistor is the highest in this region.

But, in subthreshold region, transistor size will become huge to support the same current, the capacitance from the transistors will be very large, the pole frequency will drop dramastically. The speed of the transistor will be lowest in the region.

You can actually find a V_{ov} that with highest effeciency and pole frequecy product, they will be covered in EE240A.