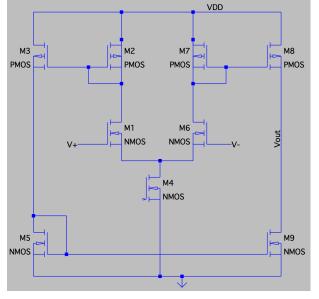
Homework Assignment #7

Due by online submission Wednesday 10/23/2019 (9am Thursday)

- 1. You have a two-stage CMOS amplifier driving an output load of 10pF. The second stage has a transconductance of 10mS, an output resistance of 10k Ω , and an input capacitance of 1pF. The first stage has a transconductance of 1mS and an output resistance of 100k Ω . Assumce C_c=0.
 - a. Draw a Bode plot of the gain and phase of the first and second stage individually, and the combined gain and phase.
 - b. Is the amplifier stable in unity gain feedback?
 - c. Estimate the largest feedback factor and corresponding gain for which the amplifier has 45 degree phase margin.
 - Now we will add C_c to make the amplifier stable in unity gain feedback.
 - d. Assuming that C_c will be bigger than C_1 , estimate the second stage pole.
 - e. Ignoring the RHP zero from C_c and the pole/zero doublet from the current mirror, where do you need to put the unity gain frequency in order to get a 45 degree phase margin in unity gain feedback?
 - f. What is the value of Cc which achieves this? Was your assumption correct in part d?
 - g. Where is the compensated first stage pole?
 - h. Draw a Bode plot of the compensated amplifier.
- 2. Check out the "early op-amp" in Figure 2 on this page <u>https://www.maximintegrated.com/en/app-notes/index.mvp/id/4428</u>.
 - a. Circle and label the following components
 - i. differential pair with resistive load
 - ii. tail current sink
 - iii. common emitter gain stage with level-shifting diodes
 - iv. output stage with current-limiting resistors
 - v. Zener diode based voltage reference
 - b. Why is there a resistor in series with the Zener diode?
 - c. If the Zener has a reverse breakdown of 3.5V, and the tail resistor is $1k\Omega$, what is the tail current? Does it vary much with supply voltage?
 - d. If you were going to add a compensation capacitor to this op-amp, where would you put it? (draw it on the circuit)
- 3. You have three op-amp topologies: single stage active load (our standard 5 transistor opamp), the two stage version of that, and the current mirror op-amp (schematic below). Each topology can either have NMOS or PMOS inputs, for six different flavors. Which sketch the output swing vs. common mode input range for each flavor.
- 4. The LT1008 <u>http://cds.linear.com/docs/en/datasheet/1008fb.pdf</u> (also decades old, \$3.55 on digikey) is not internally compensated. This gives you higher performance (BW, slew rate) for higher gain, but means that you need to add external capacitance when using the amplifier in low-gain configurations. They give you two choices, either add a capacitor C_F that will be somewhat Millerized or add C_S that looks more like our C₂.
 - a. with a closed loop gain of 1,000 and perfect feedback resistor matching,
 - i. estimate your gain error at 0.1 Hz
 - ii. estimate the closed-loop pole location with $C_S=10$ pF vs. $C_F=30$ pF (page 6, lower left)
 - b. With CF=3pF vs. 30pF, what is the maximum feedback factor (and corresponding minimum gain and max bandwidth) that will give a phase margin of 60? (page 6, lower right)
- 5. Figure 6.15 in Razavi is a model of a two-stage amplifier. [For ee247A students: Fig 9.18 in GHLM, and equations 9.27 and 9.33 for parts b and c]
 - a. re-draw it using our terminology from class: Gm1, Gm2, Ro1, Ro2, C1, C2, Cc.
 - b. Equation 6.30 is the transfer function of the amplifier. Re-write that with our terminology.

- c. Equation 6.39 is the simplified expression for the 2nd pole location, assuming the first pole is given by Miller-multiplied Cc.
 - i. Re-write that with our terminology
 - ii. Assuming that the 2nd stage gain is much larger than 1, the Miller capacitance is all that matters in the compensated first stage pole $\omega_{p1,c}$, write the expression for the compensated second stage pole $\omega_{p2,c}$ in terms of only capacitors and the transconductance of the second stage.
 - iii. With those same assumptions, and ignoring any other poles and zeros, what is the constraint on transconductance and capacitance that insures a unity gain phase margin of at least 45?
- 6. [240A] In the "early op-amp" above,
 - a. if the current-limiting resistors are small, estimate the gain of the output stage as a function of output current to/from the load
 - b. if the two diodes are implemented as diode-connected versions of the two output transistors, the current limiting resistors are 10 Ohms, and the output is grounded (or connected to a very low impedance load to ground), sketch the output current as a function of the collector voltage on the common emitter gain stage, over a +/-2V range.



Current mirror op-amp