# EE 140/240A Linear Integrated Circuits
# Fall 2019 Homework 7

## 1. Compensation for Stability

You have a two-stage CMOS amplifier driving an output load of $C_2 = 10\text{pF}$. The second stage has a transconductance of $G_{m2} = 10\text{mS}$, an output resistance of $R_{o2} = 10\text{k}\Omega$, and an input capacitance of $C_1 = 1\text{pF}$. The first stage has a transconductance of $G_{m1} = 1\text{mS}$ and an output resistance of $R_{o1} = 100\text{k}\Omega$.

(a) Draw a Bode plot of the gain and phase of the first and second stage individually, and the combined gain and phase.

**Solution:**

$$\begin{aligned} A_{v0,1} &= -G_{m1}R_{o1} \\ &= -1\cdot 10^{-3}\cdot 10^{5} \\ &= -100 \end{aligned}$$

$$\begin{aligned} A_{v0,2} &= -G_{m2}R_{o2} \\ &= -10\cdot 10^{-3}\cdot 10\cdot 10^{3} \\ &= -100 \end{aligned}$$

Note the initial phase!

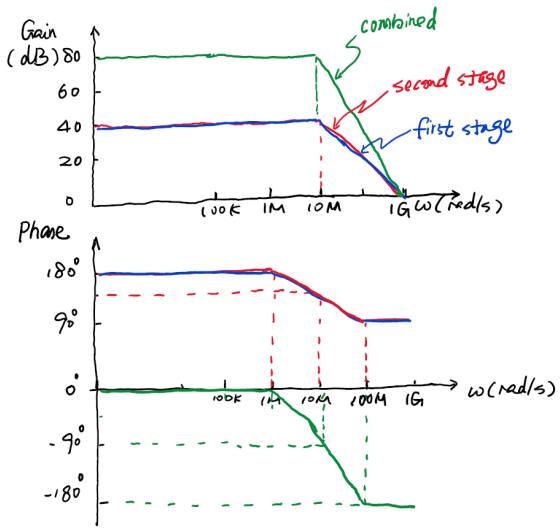
Again, note the negative sign, so the initial phase is 180°

$$\begin{aligned} \omega_{p1} &= \frac{1}{R_{o1}C_1} \\ &= \frac{1}{100\cdot 10^{3}\cdot 1\cdot 10^{-12}} \\ &= \frac{1}{10^{-7}} \\ &= 10\text{Mrad/s} \end{aligned}$$

$$\begin{aligned} \omega_{p2} &= \frac{1}{R_{o2}C_2} \\ &= \frac{1}{10\cdot 10^{3}\cdot 10\cdot 10^{-12}} \\ &= \frac{1}{10^{-7}} \\ &= 10\text{Mrad/s} \end{aligned}$$

Combined, the pole locations don't change (because the poles aren't in any feedback or feedforward loop), and we simply need to find the gain:

$$\begin{aligned} A_{v0} &= A_{v0,1}A_{v0,2} \\ &= 10^{4} \end{aligned}$$




**Rubric:** (6 Points)

- +2: Correct plot for magnitude, phase of $A_{v1}$, $A_{v2}$, and $A_v$ ($3\times$)

(b) Is the amplifier stable in unity gain feedback?

**Solution:**

Marginal stable or not stable—the amplifier just reaches $-180°$ at the unity gain frequency.

**Rubric:** (2 Points)

- +2: Correct answer of marginally stable or not stable (either is acceptable)

(c) Estimate the largest feedback factor and corresponding gain for which the amplifier has 45° phase margin.

**Solution:** [2pts]

Consider the plot of $A_0(s)f$. We to find $f$ such that the phase margin of $A_0 f$ at unity gain is 45 degrees. Given $A_0(s)$, we want the unity gain frequency of $A_0 f$ to be no more than half a decade higher than $10^7$rad/s, and $A_0$ is 60dB at that frequency. Thus, $f \leq \frac{1}{1000}$

**Rubric:** (2 Points)

- +1: Correct feedback factor
- +1: Correct corresponding gain

(d) Now we will add $C_C$ to make the amplifier stable in unity gain feedback.
Assuming that $C_C$ will be bigger than $C_1$, estimate the second stage pole.

**Solution:** [2pts]

$$\begin{aligned}\omega_{p2,C} &= -\frac{G_{m2}C_C}{C_CC_1 + C_1C_2 + C_CC_2} \\ &\approx \frac{G_{m2}}{C_2} \\ &= 1\text{Grad/s}\end{aligned}$$

$$\omega_{p2,C} \approx 1\text{Grad/s}$$

**Rubric:** (2 Points)

- +2: Correct estimate of second stage pole

(e) Ignoring the right-half plane zero from $C_C$ and the pole/zero doublet from the current mirror, where do you need to put the unity gain frequency in order to get a 45° phase margin in unity gain feedback?

**Solution:** [2pts]

To have a 45° phase margin, the unity gain frequency should be made equal to $\omega_{p2,C}$ (calculated above.)

$$\omega_u = \omega_{p2,C} \approx 1\text{Grad/s}$$

**Rubric:** (2 Points)

- +2: Correct unity gain frequency

(f) What is the value of $C_C$ which achieves this? Was the assumption correct in part (d)?

**Solution:**

$$\begin{aligned}\omega_{p2,C} &= \omega_u \\ \frac{G_{m2}}{C_2} &= \frac{G_{m1}}{C_C} \\ C_C &= \frac{G_{m1}}{G_{m2}}C_2 \\ &\approx 1\text{pF}\end{aligned}$$

$$C_C \approx 1\text{pF}$$

The assumption that $C_C > C_1$ was not correct, meaning we'd need a larger $C_C$ to get the phase margin as what we want.

**Rubric:** (2 Points)

- +1: Correct compensation capacitor
- +1: Correctly stated that assumption in previous part was incorrect

(g) Where is the compensated first stage pole?

**Solution:** [2pts]

$$\begin{aligned}\omega_{p1,C} &\approx \frac{1}{R_{o1}G_{m2}R_{o2}C_C} \\ &= 100\text{krad/s}\end{aligned}$$

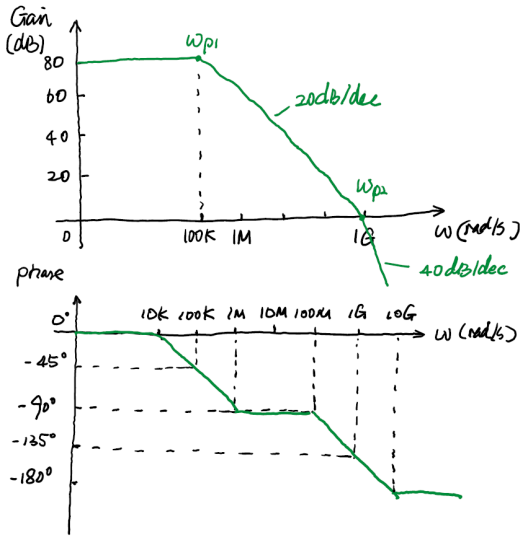
$$\omega_{p1,C} \approx 100\text{krad/s}$$

**Rubric:** (2 Points)

- +2: Correct compensated first stage pole

(h) Draw a Bode plot of the compensated amplifier.

**Solution:** [2pts]




**Rubric:** (2 Points)

- +1: Correct magnitude plot
- +1: Correct phase plot

**2. Early Op Amp** Check out the "early op-amp" figure from Maxim Integrated (included below for convenience)

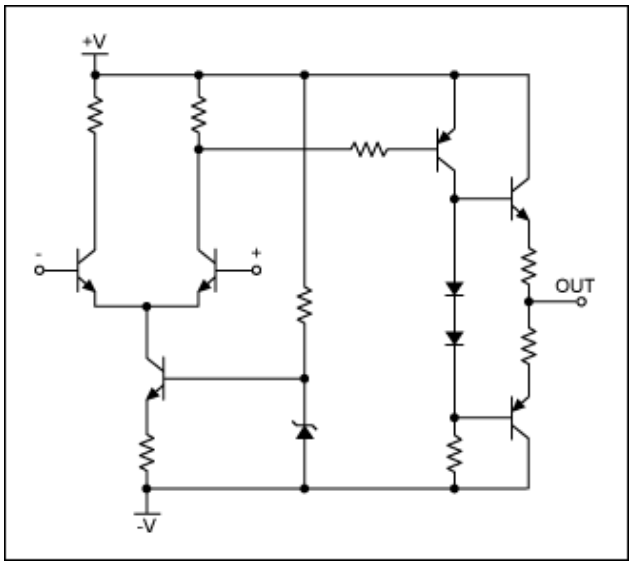
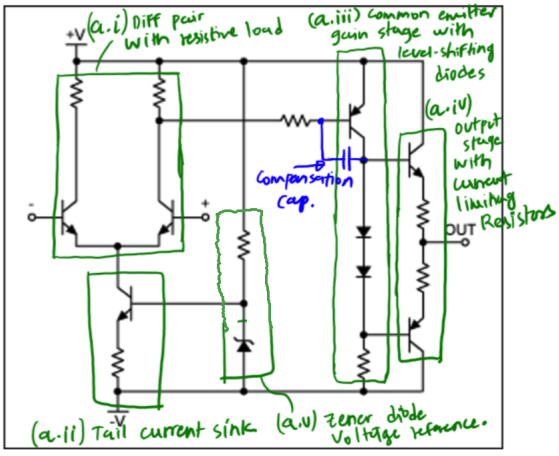



Figure 1: Source: https://www.maximintegrated.com/en/app-notes/index.mvp/id/4428

(a) Circle and label the following components:

i. differential pair with resistive load
ii. tail current sink
iii. common emitter gain stage with level-shifting diodes
iv. output stage with current-limiting resistors
v. Zener diode based voltage reference

**Solution:**




**Rubric:** (5 Points)

- +1: Per correct answer (5×)

(b) Why is there a resistor in series with the Zener diode?

**Solution:**

The series resistor supplies current to the zener to run it in reverse breakdown, also limits current through the Zener diode.

**Rubric:** (1 Points)

- +1: Series resistor limits current (saying that it supplies current to the Zener so it runs in reverse breakdown is also acceptable).

(c) If the Zener has a reverse breakdown of 3.5V, and the tail resistor is 1kΩ, what is the tail current? Does it vary much with supply voltage?

**Solution:**

$$\begin{aligned} I_{\text{TAIL}} &= \frac{V_{\text{Zener}} - V_{BE}}{R_{\text{TAIL}}} \\ &= \frac{3.5 - 0.7}{1000} \\ &\approx 2.8\text{mA} \end{aligned}$$

$I_{\text{TAIL}} \approx 2.8\text{mA}$

Neiher $V_{\text{Zener}}$ nor $V_{BE}$ depend on the supply voltage, hence, the tail current is relatively independent of supply.

**Rubric:** (2 Points)

- +1: Correct calculation of tail current
- +1: Correct explanation of no dependence on supply voltage

(d) If you were going to add a compensation capacitor to this op-amp, where would you put it? (draw it on the circuit)

**Solution:**

See (a).

**Rubric:** (1 Points)

- +1: Correct placement of compensation capacitor. Placement from the input of the common emitter to the output is also acceptable.

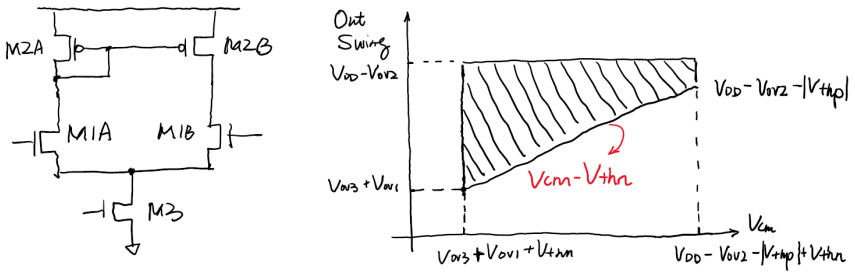
## 3. Output Range

You have three op-amp topologies: single stage active load (our standard 5 transistor opamp), the two stage version of that, and the current mirror op-amp (schematic below). Each topology can either have NMOS or PMOS inputs, for six different flavors. Which sketch the output swing vs. common mode input range for each flavor.

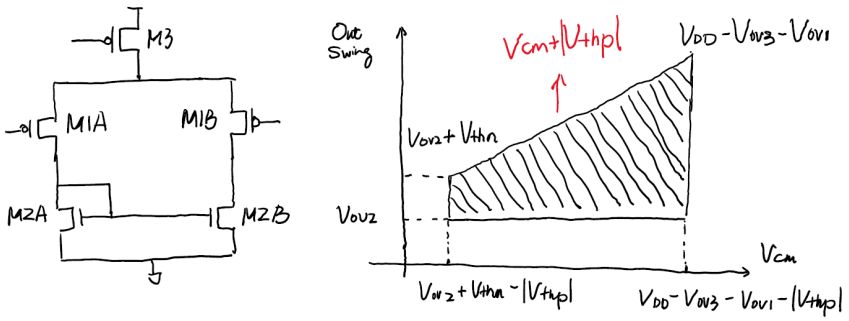
**Rubric:** (12 Points)

- +2: Per correct amplifier $(6\times)$

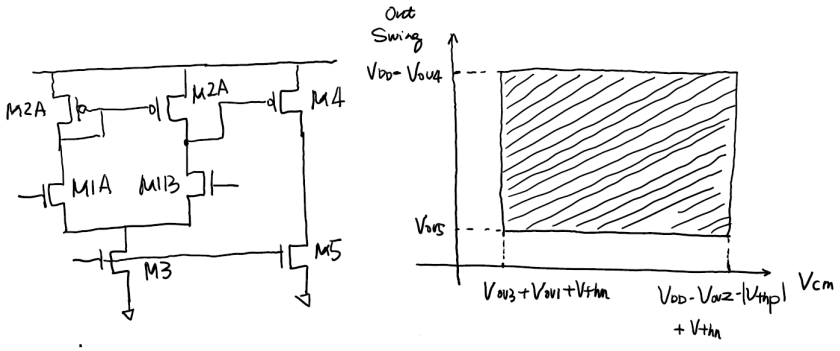
**Solution:** 5 transistor opamp with nmos input:



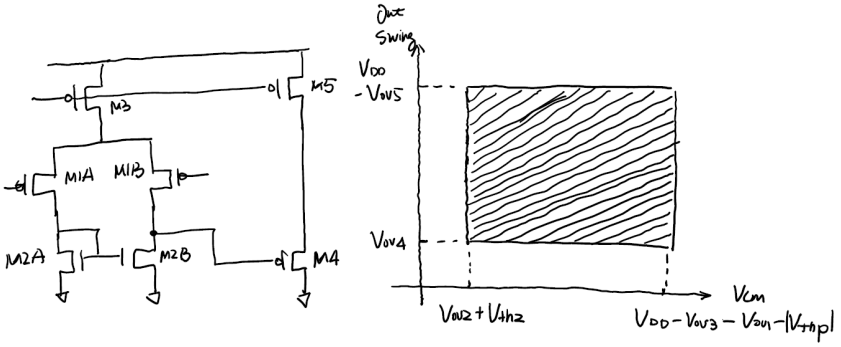

5 transistor opamp with pmos input:



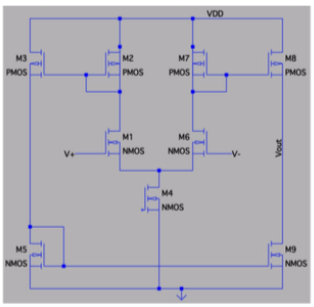

two-stage opamp with nmos input (in the exam, you can just assumme $V_{ov4}$ is constant and use this answer):

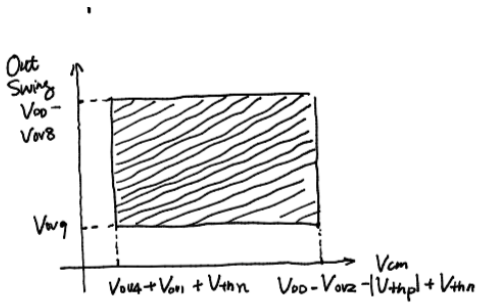



two-stage opamp with pmos input (in the exam, you can just assumme $V_{ov4}$ is constant and use this answer):

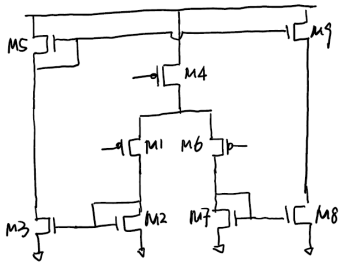


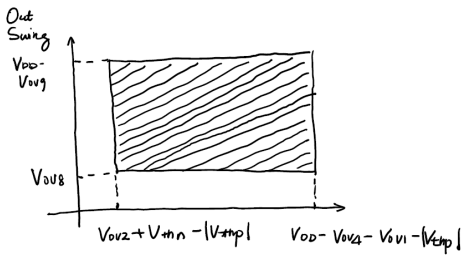
current mirror opamp with nmos input (in the exam, you can just assumme $V_{ov4}$ is constant and use this answer):




current mirror opamp with pmos input (in the exam, you can just assumme $V_{ov4}$ is constant and use this answer):




## 4. LT1008

The LT1008 (https://www.analog.com/media/en/technical-documentation/data-sheets/LT1008.pdf) is also decades old, but it is not internally compensated. This gives you higher performance (bandwidth, slew rate) for higher gain, but it means you have to add external capacitance when using the amplifier in low-gain configurations. They give you two choices: either add a capacitor $C_F$ that will be somewhat Millerized or add $C_S$ that looks more like our $C_2$.

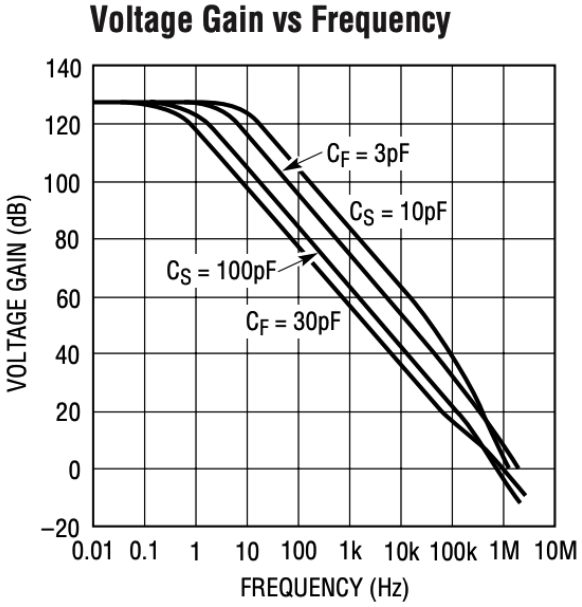
(a) With a closed loop gain of 1000 and perfect feedback resistor matching,

i. estimate your gain error at 0.1Hz

ii. estimate the closed-loop pole location with $C_S = 10$pF vs. $C_F = 30$pF (page 6, lower left)

**Solution:**

At $f = 0.1Hz$, the DC gain $A_{vo} = 130dB$ and 3.2M. As closed-loop gain $A_{vc} = 1000$, loop gain $Af = A_{vo}/A_{vc} = 3.2K$. Then fractional gain error is $1/3.2K = 31.3e-3$.




For $C_S = 10pF$, open-loop pole is $\omega_{3dB} = 5Hz$. The closed-loop pole is $3.2K \cdot 5 = 16KHz$.
For $C_F = 10pF$, open-loop pole is $\omega_{3dB} = 0.2Hz$. The closed-loop pole is $3.2K \cdot 0.2 = 640Hz$.

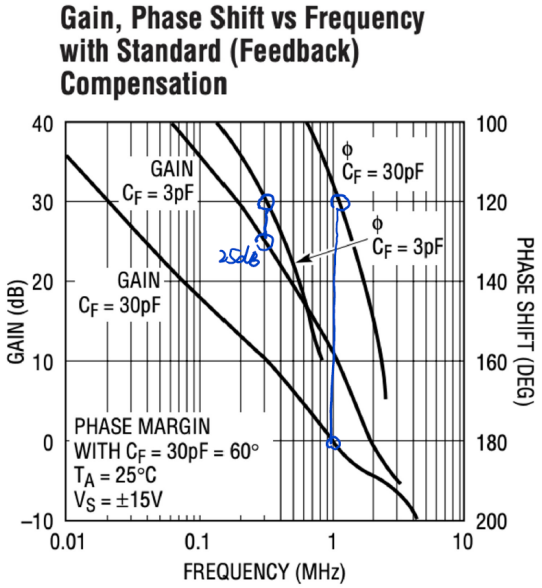
**Rubric:** (3 Points)

- +1: Correct gain error
- +1: Per correct pole (2×)

(b) With $C_F = 3$pF vs. 30pF, what is the maximum feedback factor (and corresponding minimum gain and max bandwidth) that will give a phase margin of 60? (page 6, lower right)

**Solution:**

For $C_F = 3pF$, closed-loop gain $A_{vc} = 25dB \approx 15\frac{\text{V}}{\text{V}}$. Then, the maximum feedback factor $f = 1/A_{vc} \approx \frac{1}{15}$, with maximum bandwidth 300KHz.
For $C_F = 30pF$, closed-loop gain $A_{vc} = 0dB = 1$. Then, the maximum feedback factor f=1, with maximum bandwidth 1MHz.



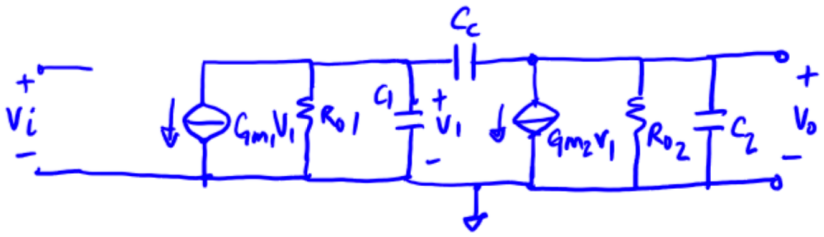
**Rubric:** (4 Points)

- +1: Per correct gain (2×)
- +1: Per correct bandwidth (2×)

## 5. Razavi's equations

Figure 6.15 in Razavi is a model of a two-stage amplifier. [For ee247A students: Fig 9.18 in GHLM, and equations 9.27 and 9.33 for parts b and c]

(a) Re-draw it using our terminology from class: $G_{m1}$, $G_{m2}$, $R_{o1}$, $R_{o2}$, $C_1$, $C_2$, $C_c$.
**Solution:**




**Rubric:** (2 Points)

- +2: Correct

(b) Equation 6.30 is the transfer function of the amplifier. Re-write that with our terminology.
**Solution:** [2 pts]

$$\frac{V_o(s)}{V_i(s)} = \frac{(C_c s - G_{m2}) R_{o2}}{R_{o1}R_{o2}\zeta_1 s^2 + R_{o1}\left((1+G_{m2}R_{o2})C_c + C_1\right) + R_{o2}(C_c+C_2)s + 1}$$

where, $\zeta_1 = C_1C_c + C_1C_2 + C_cC_2$

**Rubric:** (2 Points)

- +2: Correct rewrite

(c) Equation 6.39 is the simplified expression for the 2nd pole location, assuming the first pole is given by Miller-multiplied $C_c$.

i. Re-write that with our terminology
**Solution:** [1 pts]

$$\omega_{p2} = \frac{1}{\omega_{p1}} \frac{1}{R_{o1}R_{o2}(C_1C_2+C_1C_c+C_2C_c)} = \frac{R_{o1}[(1+G_{m2}R_{o2})C_c+C_1]+R_{o2}(C_c+C_2)}{R_{o1}R_{o2}(C_1C_2+C_1C_c+C_2C_c)}$$

ii. Assuming that the 2nd stage gain is much larger than 1, the Miller capacitance is all that matters in the compensated first stage pole wp1,c, write the expression for the compensated second stage pole wp2,c in terms of only capacitors and the transconductance of the second stage.
**Solution:** [1 pts]

$$\omega_{p2} \approx \frac{G_{m2}}{C_2}$$

iii. With those same assumptions, and ignoring any other poles and zeros, what is the constraint on transconductance and capacitance that insures a unity gain phase margin of at least 45?
**Solution:** [1 pts]
To make $PM \geq 45°$, $\omega_u \leq \omega_{p2}$. Then,

$$\frac{G_{m2}C_c}{G_{m1}C_2} \geq 1$$

**Rubric:** (3 Points)

- +1: Per correct subpart

**6. Early Op Amp** [6 pts]

[240A] In the "early op-amp" above,

(a) if the current-limiting resistors are small, estimate the gain of the output stage as a function of output current to/from the load

**Solution:** [2 pts]

Only one of the two transistors is on, then

$Av = \frac{g_m r_o}{1+g_m r_o}, g_m = \frac{I_{out}}{V_t}$

**Rubric:** (2 Points)

- +2: Correct

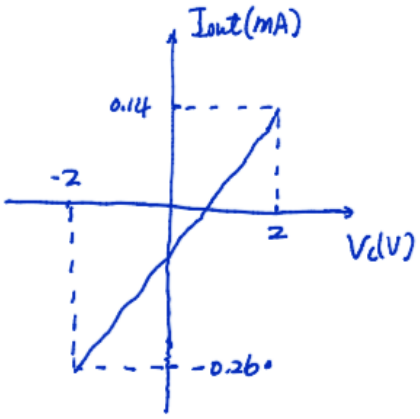
(b) if the two diodes are implemented as diode-connected versions of the two output transistors, the current limiting resistors are 10 Ohms, and the output is grounded (or connected to a very low impedance load to ground), sketch the output current as a function of the collector voltage on the common emitter gain stage, over a +/-2V range.

**Solution:** [4 pts, 1 for two currents each, 2 for the figure]

When $V_c = 2V$, $I_{out} = \frac{2-0.6}{10} = 0.14mA$

When $V_c = -2V$, $I_{out} = \frac{-2-1.2+0.6}{10} = -0.26mA$

You can also use 0.7 for $v_{be}$ in your solutions.




**Rubric:** (4 Points)

- +1: Correct current (2×)
- +2: Correct figure