## Homework Assignment \#8

Due by online submission Wednesday 10/30/2019 (9pm hard deadline)

1. 2015 spring Midterm 2, Question 4 (except 4e) (compensation of OPA334)
2. 2015 spring Midterm 2, Question 6 (DC design of 2 stage)
3. 2015 spring Midterm 2, Question 7 (should be 2015, plot magnitude of 2 stage gains)
4. 2017 spring Midterm 2, Question 2 (single pole in feedback)
5. 2017 spring Midterm 2, Question 3 (bandgap)
6. Calculate the common mode gain for the first stage of your op-amp from lab3 part 1.
7. For each of the following four op-amps, redraw the schematic of the op-amp including only those transistors that are on when the op-amp is slewing positive, and then slewing negative. (there should be 8 figures: 2 topologies, 2 types of input transistors, 2 slewing directions)
a. our standard 5T single-stage CMOS op-amp, with NMOS input, and with PMOS input
b. the current mirror op-amp, with NMOS, and with PMOS
8. For a two-stage NMOS-input CMOS op-amp with the output stage biased at 10 uA and the tail current at 1 uA
a. calculate the positive and negative slew rate if $\mathrm{C}_{\mathrm{c}}=1 \mathrm{pF}$ and $\mathrm{C}_{\mathrm{L}}=1 \mathrm{pF}$.
b. calculate the positive and negative slew rate if $\mathrm{C}_{\mathrm{c}}=1 \mathrm{pF}$ and $\mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$.
9. In the circuit below
a. What do we call the amplifier configuration of transistors M10 and M11?
b. Does this additional amplifier prevent or enable Cc from being useful as a Miller compensation capacitor?
c. What effect does this additional amplifier have on the right-half plane zero normally present with Miller compensation? Why?
d. What effect, if any, does this additional amplifier have on the input common mode range and output swing?

10. Take a look at the datasheet for the TI LM324 quad op-amp.
http://www.ti.com/lit/ds/symlink/lm324.pdf TI has been selling this op-amp for more than 40 years! (they are 10 cents each on digikey) From Figure 4 on the LM324 datasheet
a. estimate the slew rate in positive and negative slewing when the output load is 50 pF
b. we haven't studied output stages, but you can find the output current limits in the table on page 7. Is the slew rate due to the output capacitor? (hint: no. Explain why.)
c. What else could it be then? Estimate the size of the compensation capacitor $\mathrm{C}_{\mathrm{c}}$
11. For a two-stage NMOS-input CMOS op-amp with the output stage biased at 10 uA and the tail current at 1 uA with $\mathrm{C}_{\mathrm{c}}=1 \mathrm{pF}$ and $\mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$., assume a 5 V supply, 1 V threshold voltages, and 100 mV overdrive voltages for all transistors. With the op-amp in unity gain feedback,
a. on a single plot carefully sketch the output voltage of the first and second stage vs. time when the input makes a step change from 2 V to 4 V . Your plot should clearly show initial and final values, and rates of change. Calculate the rate of change of the voltage on Cc. You only need to show the slewing behavior, but estimate the voltage and time at which the op-amp stops slewing.
b. repeat, for an input transition from 4 V to 2 V .
