# EE 140/240A $\,$ Linear Integrated Circuits Fall 2019

1

# 1. (Spring 2015 Midterm 2 Q4)

The TI OPA334 is a single-ended CMOS op-amp similar to what you've been designing in class. The frequency response from the datasheet is shown below.



(a) What is the open loop gain? **Solution:** 

This is approximately half a decade above  $10^6$ , so  $3 \times 10^6 V/V$ 

**Rubric:** (2 Points)

- +2: Correct open loop gain (acceptable to estimate as half on the log scale or linear scale)
- (b) What is the lowest frequency pole? **Solution:**

 $f_{3dB} \approx 0.8 \text{Hz}$ 

**Rubric:** (2 Points)

• +2: Correct pole frequency

# (c) What is the phase margin? Solution:

 $\phi_{PM} \approx 80^{\circ}$ 

Rubric: (2 Points)

• +2: Correct phase margin

(d) Is the amplifier unity-gain stable? **Solution:** 

Yes

**Rubric:** (2 Points)

• +2: Correct answer

# 2. (Spring 2015 Midterm 2 Q6)

In the two-stage op-amp below, assuming  $I_{ref} = 10\mu A$  and  $(W/L)_6 = 10\mu m/1\mu m$ , design the amplifier so that the tail current is  $20\mu A$ , the second stage current is  $100\mu A$ , and the PMOS devices have  $V_{ov} = 100mV$ .

Process specs:

•  $\mu_n C_{ox} = 2\mu_p C_{ox} = 200\mu A/V^2$ •  $\lambda = 1/(10V)$ •  $V_{tn} = -V_{tp} = 0.5V$ •  $V_{DD} = 2V$ •  $L_{min} = 1\mu m$ •  $C_{ox} = 5fF/\mu m^2$ •  $C'_{ol} = 0F/\mu m$ 



2

| $(W/L)_1$ |          | $g_{m1}$ |  |
|-----------|----------|----------|--|
| $(W/L)_2$ |          | $R_{o1}$ |  |
| $(W/L)_3$ |          | $g_{m4}$ |  |
| $(W/L)_4$ |          | $R_{o2}$ |  |
| $(W/L)_5$ |          | $A_{v1}$ |  |
| $(W/L)_6$ | 10µm/1µm | $A_{v2}$ |  |

**Solution:** Our spec is quite straightforward, but the point of this question was more so making sure students knew how to find the important small signal parameters of an amplifier they designed. Here goes!

- (a) Tail current is 20µA: Given that  $I_{ref} = 10\mu A$ , we know that M3 = 2M6  $\rightarrow (W/L)_3 = 20\mu m/1\mu m$
- (b) Second stage current is 100µA: Similar to what we did for M3, we'll do for M5, so M5 = 10M6  $\rightarrow (W/L)_5 = 100\mu m/1\mu m$
- (c) PMOS devices have  $V_{ov} = 100$ mV: This means  $V_{G2}$  and  $V_{G4}$  are equal (which makes sense for matching with the current mirror load) and are at a particular voltage  $V_{DD} |V_{tn}| V_{ov} \longrightarrow V_{G2} = V_{G4} = 1.4$ V
- (d) Now calculating the size of the PMOS devices to sink the appropriate amount of current given our overdrive

$$\frac{W}{L} = \frac{2I_D}{\mu_p C_{ox} V_{oy}^2}$$

$$\rightarrow (W/L)_2 = 20 \mu m/1 \mu m, (W/L)_4 = 200 \mu m/1 \mu m$$

(e) At this point, we're almost finished! It just becomes a question of what overdrive voltage we want to drive our input pair at. For the sake of this problem, we can go with something fairly small like 100mV to size our input devices  $\longrightarrow (W/L)_1 = 10 \mu m/1 \mu m$ 

Our equations of interest after all of that are as follows:

$$g_m = \frac{2I_D}{V_{ov}}$$

$$r_o = \frac{1}{\lambda I_D}$$

$$R_{o1} \approx r_{o2B} ||r_{o1B}$$

$$R_{o2} \approx r_{o4} ||r_{o5}$$

| $\begin{array}{c cccc} (W/L)_2 & 20\mu m/1\mu m \\ \hline (W/L)_3 & 20\mu m/1\mu m \\ \hline (W/L)_4 & 200\mu m/1\mu m \\ \hline (W/L)_5 & 100\mu m/1\mu m \\ \hline A_{-1} & -100 \\ \hline \end{array}$ |
|---|
| $\begin{array}{c cccc} (W/L)_3 & 20\mu m/1\mu m \\ \hline (W/L)_4 & 200\mu m/1\mu m \\ \hline (W/L)_5 & 100\mu m/1\mu m \\ \hline A_{-1} & -100 \\ \hline \end{array}$                                    |
| $\frac{(W/L)_4}{(W/L)_5} \frac{200 \mu m/1 \mu m}{100 \mu m/1 \mu m} = \frac{R_{o2}}{4 \mu m} \frac{50 k \Omega}{100 \mu m/1 \mu m}$  |
| $(W/L)_{5} = 100 \mu m/1 \mu m$ $A_{v1} = -100$   |
|   |
| $(W/L)_6$ 10µm/1µm $A_{\nu 2}$ -100   |

**Rubric:** (28 Points)

- +1: Correct approach for finding W/L of device ( $\times$ 7)
- +1: Correct numerical value for W/L of device ( $\times$ 7)

- +1: Correct approach for each of  $g_m$ ,  $R_o$ , and  $A_v$  calculation (×6)
- +1: Correct numerical value for each of  $g_m$ ,  $R_o$ , and  $A_v$  (×6)
- +2: Some indication that  $I_D$  through each M2 and M1 should be  $10\mu A$  (half the tail current)

# 3. (Spring 2015 Midterm 2 Q7)



A design of the 2-stage op-amp above has the following parameters

| $g_{m1}$ | $R_{o1}$ | $g_{m4}$ | $R_{o2}$ | $C_2$ | $C_C$ | $C_{gs4}$ |
|----------|----------|----------|----------|-------|-------|-----------|
| 1µS      | 100MΩ    | 10µS     | 100MΩ    | 1pF   | 10fF  | 100fF     |

(a) What are the uncompensated ( $C_C = 0$ ) DC gain and pole locations of the two stages? **Solution:** First the pole locations

$$\begin{split} \omega_{p1} &= \frac{1}{R_{o1}C_{1}} & \omega_{p2} &= \frac{1}{R_{o2}C_{2}} \\ &\approx \frac{1}{100 \cdot 10^{6} \cdot 100 \cdot 10^{-15}} & = \frac{1}{100 \cdot 10^{6} \cdot 1 \cdot 10^{-12}} \\ &= \frac{1}{10^{2+6+2-15}} & = \frac{1}{10^{2+6-12}} \\ &= \frac{1}{10^{-5}} & = \frac{1}{10^{-4}} \\ &= 100 \text{ krad/s} \end{split}$$

And then the gain

$$A_{v1} = -g_{m1}R_{o1} \qquad A_{v2} = -g_{m4}R_{o2} \\ = -1 \cdot 10^{-6} \cdot 100 \cdot 10^{6} \qquad = -10 \cdot 100 \\ = -100 \qquad = -1000$$

 $\omega_{p1} = 100$ krad/s  $\omega_{p2} = 10$ krad/s  $A_{v1} = -100$  $A_{v2} = -1000$ 

(b) Now reinsert  $C_C$  from the table. What is the frequency of the RHP zero? Assume  $R_z = 0\Omega$ . Solution:

$$\omega_{z,RHP} = \frac{g_{m2}}{C_C}$$
$$= 1 \text{Grad/s}$$

$$\omega_{z,RHP} = 1$$
Grad/s

(c) On the next page, on the top axes plot the magnitude of the impedance of  $C_1$ ,  $C_C$  by itself, and the total impedance seen at the first stage output.

Rubric: (5 Points)

- +1: Correct  $|Z_{C1}|$
- +1: Correct low-frequency  $|Z_{C_c}|$
- +1: Correct transition points for  $Z_{C_c}$
- +1: Correct high-frequency  $|Z_{C_c}|$
- +1: Correct total  $|Z_{o1}|$
- (d) On the middle axes plot the magnitude of the compensated first and second stage gains, and the overall gain. You may assume that the value of  $R_z$  has been chosen to place the RHP zero at infinity. **Rubric:** (3 Points)
  - +1: Correct  $|A_{v1}|$  given  $Z_{o1}$  from previous part (don't double-penalize)
  - +1: Completely correct  $|A_{\nu 2}|$
  - +1: Correct cumulative gain
- (e) On the bottom axes plot the phase of the overall gain.

**Rubric:** (2 Points)

- +1: Correct phase transition about first pole
- +1: Correct phase transition about second pole



6

# **Solution:**



# 4. (Spring 2017 Midterm 2 Q2)

A single-pole amplifier has a gain of 1,000 and a pole at 1MHz. It is used in feedback with a feedback factor f = 0.01. Calculate the following:

(a) Approximate closed-loop gain

Solution:

$$A_{\rm CL} \approx \frac{1}{f}$$
$$= 100 {\rm V/V}$$

$$A_{\rm CL} \approx 100 {\rm V}/{\rm V}$$

**Rubric:** (2 Points)

- +1: Correct equation  $\frac{1}{f}$
- +2: Correct numerical value
- (b) Percent gain error **Solution:**

$$-\frac{1}{Af} \times 100\% = -\frac{1}{1000 \cdot 0.01} \times 100\%$$
$$= -0.1 \times 100\%$$
$$= -10\%$$

percent gain error = -10%

**Rubric:** (2 Points)

- +1: Correct equation  $-\frac{1}{Af}$
- +2: Correct numerical value
- (c) Closed-loop pole location **Solution:**

$$f_{p,\text{CL}} = \frac{\text{GBW}}{A_{\text{CL}}}$$
$$= 10\text{MHz}$$

$$f_{p,\text{CL}} = 10\text{MHz}$$

**Rubric:** (2 Points) • +1: Correct equation  $\frac{\text{GBW}}{A_{\text{CL}}}$ 

- +2: Correct numerical value
- (d) Time constant of the step response **Solution:**

$$\tau = \frac{1}{\omega_{p,\text{CL}}}$$
$$= \frac{1}{2\pi f_{p,\text{CL}}}$$
$$= \frac{10^{-7}}{2\pi} \text{s}$$

$$\tau = \frac{10^{-7}}{2\pi} s$$

Rubric: (2 Points)

- +1: Correct equation  $\frac{1}{\omega_{p,CL}}$
- +2: Correct numerical value

# 5. (Spring 2017 Midterm 2 Q3)

A particular diode D1 has a saturation current of 1pA, and at 1mA current at room temperature the diode voltage has a temperature coefficient of -2mV/K. You are using copies of this diode to make a bandgap reference, with D2 composed of **seven** copies of D1. You can use the approximation that  $\ln(7) \approx 2$ . Assuming that the current in both diodes is maintained at 1mA at room temperature,



#### **Rubric:** (6 Points)

- +2 for parts a, b, d, e no partial credit.
- +3 for part c.
- +9 for part f, +3 per line/function

• +2 for part g.

(a) What is the voltage on D1 at room temperature?Solution: Between 1pA and 1mA there are 9 decades, so

9 decades  $\cdot$  60mV = 0.54V

## 0.54V

(b) What is the voltage on D2 at room temperature? Solution: The voltage is a factor of  $\ln(7)V_T$  smaller than that across D1, so

```
0.54V - 2 \cdot 26mV \approx 0.49V
```

#### 0.49V

(c) What is the difference between the two diode voltages at 200K, 300K, and 400K? Solution: The difference scales with  $V_T = \frac{k_B T}{q}$ 

> @200K:35mV @300K:52mV @400K:70mV

(d) What is the temperature coefficient of the voltage on D2? **Solution:** 

$$-\frac{2mV}{K}-\frac{52mV}{300K}\approx-2.17\frac{mV}{K}$$

$$\approx -2.17 \frac{\mathrm{mV}}{\mathrm{K}}$$

(e) Roughly what is the right value for *R*<sub>1</sub>? **Solution:** 

$$R_1 = \frac{52\text{mV}}{1\text{mA}}$$
$$= 52\Omega$$

 $R_1 = 52\Omega$ 

- (f) On the next page, carefully sketch by hand the voltage on D1, the voltage on D2, and the difference between them as a function of temperature from 200K to 400K.
- (g) On the same plot, if  $R_3 = R_2 = 10R_1$ , sketch  $V_{ref}$  vs. temperature from 200K to 400K.



It will help your grade if you draw carefully and label the voltage values of any dots that you draw.



# 6. Surprise, Kids! Bet You Thought You'd Seen the Last of Me!

Calculate the common mode gain for the first stage of your op-amp from lab3 part 1.

# **Solution:**

Looking to the half circuit of the first stage, we have

$$R_{o1} \approx \frac{1}{g_{m2a}}$$
$$G_{m1} \approx \frac{1}{2r_{o3}}$$

So the common mode gain is approximately

$$A_{CM} = A_{CM1}A_2 \\\approx \frac{1}{2g_{m2a}r_{o3}} \times g_{m4}(r_{o4}||r_{o5})$$

**Rubric:** (4 Points)

- +1: Correct  $R_{o1}$  for first stage
- +1: Correct  $G_{m1}$  for first stage
- +1: Correct voltage gain of second stage
- +1: Correct sign of final voltage gain

#### 7. Amps and Slewing

For each of the following four op-amps, redraw the schematic of the op amp including only those transistors that are on when the op-amp is slewing positive, and then slewing negative (there should be 8 figures: 2 topologies, 2 types of input transistors, 2 slewing directions).

(a) Our standard 5T single stage CMOS op amp with an NMOS input, and with PMOS input

# **Solution:**

Devices marked in red are on





Rubric: (12 Points)

- +1: Correct device indicated as on  $(12 \times)$
- -1: Incorrect device indicated as on (minimum 0 points)
- (b) The current mirror op-amp with NMOS and with PMOS **Solution:**

Devices marked in red are on





Rubric: (20 Points)

- +1: Correct device indicated as on  $(20 \times)$
- -1: Incorrect device indicated as on (minimum 0 points)

# 8. Two-Stages Slewing

For a two-stage NMOS-input CMOS op-amp with the output stage biased at  $10\mu A$  and the tail current at  $1\mu A$ 

(a) Calculate the positive and negative slew rate if  $C_c = 1 \text{pF}$  and  $C_L = 1 \text{pF}$ Solution:

$$I = C \frac{dV}{dt}$$
$$\frac{dV}{dt} = \frac{I}{C}$$

In each case we need to consider the possible causes of slewing. For negative slew rate, we consider two cases and assume  $A_{\nu 2} \gg 1$ :

$$-\frac{I_{\text{tail}}}{C_c} = -\frac{1\mu A}{1\text{pF}} \qquad -\frac{I_{\text{D5}}}{C_L} = -\frac{10\mu A}{1\text{pF}}$$
$$= -1 \times 10^6 \frac{\text{V}}{\text{s}} \qquad = -10 \times 10^6 \frac{\text{V}}{\text{s}}$$

We choose the most restrictive of the two (the lecture notes say the minimum of two negative values, but it should be the minimum of the *absolute value* of the two negative values).

For positive slew rate, the PMOS of the second stage can nominally provide infinite current so long as its gate is driven correctly, so the first stage + compensation capacitor limit the positive slew rate (the

compensation cap is Millerized, which removes the gain term that would come from the second stage)

$$\frac{I_{\text{tail}}}{C_c} = \frac{1\mu\text{A}}{1\text{pF}}$$
$$= 1 \times 10^6 \frac{1}{2}$$

positive rate = 
$$1 \times 10^{6} \frac{V}{s}$$
  
negative rate =  $-1 \times 10^{6} \frac{V}{s}$ 

**Rubric:** (4 Points)

- +1: Correct positive slew rate equation
- +1: Correct positive slew rate numerical value
- +1: Correct negative slew rate equation
- +1: Correct negative slew rate numerical value
- (b) Calculate the positive and negative slew rate if  $C_c = 1$  pF and  $C_L = 100$  pF **Solution:** In a similar fashion as before:

$$-\frac{I_{\text{tail}}}{C_c} = -\frac{1\mu\text{A}}{1\text{pF}} \qquad -\frac{I_{\text{D5}}}{C_L} = -\frac{10\mu\text{A}}{100\text{pF}}$$
$$= -1 \times 10^6 \frac{\text{V}}{\text{s}} \qquad = -0.1 \times 10^6 \frac{\text{V}}{\text{s}}$$

$$\frac{I_{\text{tail}}}{C_c} = \frac{1\mu\text{A}}{1\text{pF}}$$
$$= 1 \times 10^6 \frac{\text{V}}{\text{s}}$$

positive rate =  $1 \times 10^{6} \frac{V}{s}$ negative rate =  $0.1 \times 10^{6} \frac{V}{s}$ 

**Rubric:** (4 Points)

- +1: Correct positive slew rate equation
- +1: Correct positive slew rate numerical value
- +1: Correct negative slew rate equation
- +1: Correct negative slew rate numerical value

# 9. Getting Funky

In the circuit below

17



#### **Solution:**

Errata: The original amplifier had a PMOS instead of an NMOS for M11! If you noticed that it was a PMOS and stated that it was in positive feedback (and would likely have its output blow up and oscillate), give yourself full credit. If you didn't notice it was in positive feedback, see the rubrics below in red.

(a) What do we call the amplifier configuration of transistors M10 and M11? **Solution:** 

Source follower (the input is  $V_{out}$  and the output is the RHS of the compensation capacitor)

**Rubric:** (1 Points)

- +1: Identified as source follower
- +1: Common source
- (b) Does this additional amplifier prevent or enable  $C_c$  from being useful as a Miller compensation capacitor?

**Solution:** 

It enables (or rather, doesn't block) the first stage from seeing the Millerized  $C_c$ 

Rubric: (1 Points)

- +1: Correctly stated that it allowed Millerization of the compensation capacitor
- +1: Stated that this would actually enhance the Millerization with the gain of the additional common source stage

(c) What affect does this additional amplifier have on the right-half plane zero normally present with Miller compensation? Why?

# Solution:

The output stage no longer sees the feed-forward current, and so the right-half plane zero is removed! For Fall 2019, see W7L4 notes.

# **Rubric:** (1 Points)

- +1: Correctly stated that RHP zero is no longer seen since the feed-forward current is blocked.
- +1: This blocks feed-forward current and so the RHP zero is no longer seen (this assumes the sign of the common source is flipped)
- (d) What effect, if any, does this additional amplifier have on the input common mode range and output swing?

**Solution:** 

The input common mode range is not affected. For the source follower to work, the output must now be at least  $V_{tn} + V_{ov11} + V_{ov10}$ . Its upper range is not affected.

Rubric: (2 Points)

- +1: Correctly concluded effect on input common mode range
- +1: Correctly described effect on maximum output swing
- +1: Correctly decsribed effect on minimum output swing
- +1: Input common mode range is unaffected
- +1: Maximum output swing would not have been affected
- +1: Minimum output swing now has the additional condition that it can be no more than  $V_{DD} V_{ov11} + |V_{tp}|$

## 10. LM324

One more time! Take another look at the datasheet for the TI LM324 quad op-amp: http://www.ti. com/lit/ds/symlink/lm324.pdf. From Figure 4 on the datasheet:

(a) Estimate the slew rate in positive and negative slewing when the output load is 50pF. **Solution:** 

Copied from the datasheet, we're told that a load of 50pF was attached:



falling slew rate  $\approx -\frac{1.75V}{5\mu s}$  rising slew rate  $\approx \frac{2.25V}{5\mu s}$ =  $-0.35\frac{V}{\mu s}$  =  $0.45\frac{V}{\mu s}$ 

negative slew rate  $\approx -0.35 \frac{V}{\mu s}$  positive slew rate  $\approx 0.45 \frac{V}{\mu s}$ 

Rubric: (4 Points)

- +1: Correct method for calculating positive slew rate
- +1: Correct method for calculating negative slew rate
- +1: Correct numerical positive slew rate
- +1: Correct numerical negative slew rate
- (b) We haven't studied output stages, but you can find the output current limits in the table on page 7. Is the slew rate due to the output capacitor? (Hint: No. Explain why.) Solution:

The minimum output stage current is 1mA. Thus, the slew rate limit of the output stage would end up being  $\frac{1\text{mA}}{50\text{pF}} = 20\frac{\text{V}}{\mu\text{s}}$ , which is a lot larger than the values we got above!

#### **Rubric:** (2 Points)

- +1: Calculated the slew rate that would come from the output capacitor
- +1: Correctly concluded with correct reasoning that the output stage does not limit the slew rate
- (c) What else could it be then? Estimate the size of the compensation capacitor  $C_c$ .

#### **Solution:**

Well we really only have one other thing it could be (the compensation capacitor), which both by the rising and falling edges has a current limit of  $6\mu A$  from the diff pair current source. Averaging the

# rising and falling slew rates, we get

$$C = \frac{I}{\frac{dV}{dt}}$$
$$\approx \frac{6\mu A}{0.375\frac{V}{\mu s}}$$
$$\approx 16\text{pF}$$

 $C_c \approx 16 \mathrm{pF}$ 

Rubric: (2 Points)

- +1: Indicated the tail current was the limiting factor
- +1: Correct numerical value for  $C_c$

#### 11. Two-Stage Amp Transient

For a two-stage NMOS-input CMOS op-amp with the output stage biased at 10µA and the tail current at 1µA with  $C_C = 1$ pF and  $C_L = 100$ pF, assume a 5V supply, 1V threshold voltages, and 100mV overdrive voltages for all transistors. With the op-amp in unity gain feedback,

- (a) On a single plot carefully sketch the output voltage of the first and second stage vs. time when the input makes a step change from 2V to 4V. Your plot should clearly show initial and final values, and rates of change. Calculate the rate of change of the voltage on  $C_c$ . You only need to show the slewing behavior, but estimate the voltage and time at which the op amp stops slewing.
- (b) Repeat, for an input transition from 4V to 2V Solution:



As an aside, note that slewing will stop when the slope of the normal linear response exponential is equivalent to that of the slew rate. If the phase margin of the system is 45 degrees, then we know the time constant of the unity gain feedback circuit will be equal to the unity gain of the entire amplifier, at gm6/Cload (the second pole location). This can be found, since we know gm = 2Id/Vov = 10uA/.1 = 100uS, and therefore the time constant is 100e-6/100e-12 = 1us.

For back-of-the-envelope calculations, you can say that slewing stops when the differential input gets back to  $\sqrt{2}V_{ov}$  in the quadratic model and roughly  $2V_{ov}$  for the velocity saturated model. Give yourself credit if you used an answer like this.

Rubric: (10 Points)

- +2 for correct slew rate limiting ratio in part a)
- +4 for correct slew rate limiting ratio in part b)
- +2 for correct starting/ending points in part a)
- +2 for correct starting/ending points in part b).