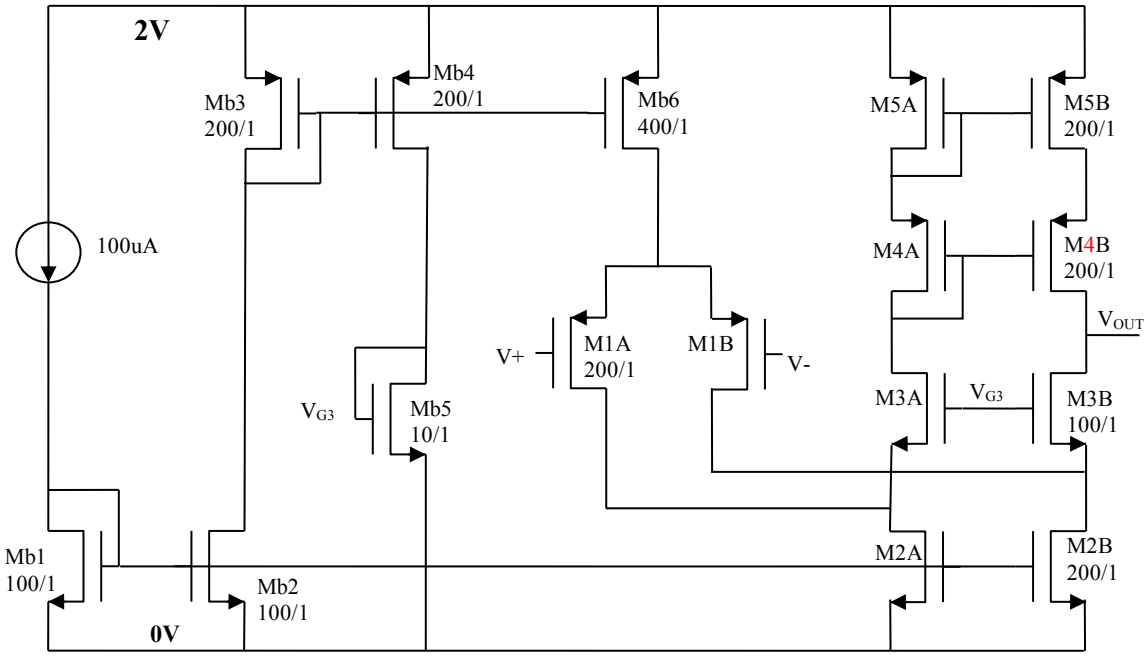
EE 140/240A Prof. Pister
Fall 2019

Homework Assignment #9

Due by online submission **Wednesday** 11/13/2019

1. Given the choice of NMOS or PMOS input stage, and the five different op-amp topologies that we've talked about (single-stage 5T diff pair with mirror load, single-stage current mirror, two-stage, telescopic cascoe, folded cascode), which combinations are appropriate for the following applications? Assume that the magnitude of the N and P threshold voltages is roughly +/-0.6V, and that all overdrive voltages are at least 0.1V.
    a. bandgap reference as in Figure 4.46c driving a 100 kΩ load
    b. digital voltage regulator with an output of 1V and a supply of between 1.6 and 3.2V
    c. analog voltage regulator with an output of 1.25V and a supply of between 1.6 and 3.2V
    d. ADC comparator with an input at 1.25V and a supply at 1.25V
    e. variable gain amplifier with an input at 0V and a supply at 1.25V
2. Design a telescopic cascode op-amp with a 2V supply, 200 uA tail current and overdrive voltages of roughly 100 mV. Assume the simplest biasing as discussed in class (3 stacked current mirrors). Use the results of your Lab 4 device characterization, and low Vt devices with 1 um channel lengths.
    a. Draw a schematic, showing device sizes and currents, and node bias points.
    b. Make a table with device gm and ro
    c. estimate the output impedance, transconductance, and gain of the op-amp
    d. plot the output swing vs. common mode input range (box plot from previous homework)
    e. could you have made this topology with regular Vt devices?
3. Repeat the previous problem but with a high-swing current mirror and input-tracking NMOS cascode biasing. Compare the gains. Why are they different?
4. Repeat the previous problem, but with regular Vt devices.
5. For the PMOS-input folded cascode op-amp below, assume the quadratic model with the following process specs $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=100\mu A/V^2$, $\lambda=1/(10V)$, $-V_{tp}=V_{tn}=0.3V$, $C_{ox}=5fF/um^2$, $C'_{ol}=0.5fF/um$.



    a. Calculate and tabulate:
        i. the overdrive voltage and current in all devices. For this step you may assume that $\lambda=0$. The simplest order may be Mb1 through Mb6, then M1 through M5.
        ii. Calculate the bias voltages on all nodes, assuming $V_{I,CM}=1V$. Specifically: tail, G2, G3, G5, G6, S3B, S4AB, and out.
        iii. the g_m and r_o parameters for M1 through M5
    b. Calculate Gm, Ro, and Av

c. Calculate the input common mode range and output swing.
d. What is the minimum voltage that could be used on the gates of M3AB to still keep M2AB in saturation? If you used that voltage, what is the new input common mode range and output swing? How would you change the size of Mb5 to achieve that voltage?
e. If the load capacitance is 1pF (roughly the same as the input capacitance),
    i. what are the pole and unity gain frequencies?
    ii. What is the phase margin in unity gain?
    iii. What are the frequencies of the pole/zero doublets from the current mirror?

6. To increase the positive output swing of the previous amplifier,
    a. redraw the PMOS current mirror M4AB, M5AB as a high-swing cascode current mirror, as in Figure 5.18b in Razavi (5.13b in the 1st edition), but PMOS.
    b. Generate V_b (V_{G4}) using something like Mb5 above, but PMOS. What current source do you use? What gate voltage biases it? What W/L do you use for all devices, and why?
    c. [240A] generate V_b from the circuit suggested in 5.19b in Razavi. What value for $(W/L)_5$ in that figure is needed?
7. In Figure 2 of this Analog Devices discussion on voltage regulators
http://www.analog.com/en/design-center/landing-pages/001/fundamentals-of-ldo-design-and-applications.html
    a. Estimate the low-frequency loop gain T= in terms of the op-amp voltage gain A_0, gm of the pass transistor, and load resistance R_L (not shown in the figure).
    b. Why does the SENSE value connect to the positive input of the op-amp? Is this positive feedback?
8. For the circuit in figure 13.43 in Razavi (6.9 in GHLM)
    a. what ratios of C_2 to C_1 are needed to make a variable gain amplifier with gain equal to any integer between 1 and 8?
    b. for a given open-loop op-amp gain A, which of the closed-loop gains above has the worst gain error? (you may assume that C_P=0)
    c. if the desired closed-loop gain accuracy is 0.4% regardless of gain setting, what is the minimum open-loop gain necessary for the op-amp?
    d. if the amplifier must settle to within 0.4% of the correct value within 10us, what is the minimum unity gain bandwidth of the op-amp?
9. [ee240A] For the folded cascode above, how does performance change
    a. if the bias current drops to 1uA and all devices are biased at roughly V_{gs}=V_t?
    b. if the bias current remains 100uA, but the length of all devices is changed to 14nm, and the widths vary from 200nm to 400nm as appropriate for a current density of 0.5mA/um? Assume that the load capacitance is comparable to the input capacitance (which is?).