## EE 140/240A Linear Integrated Circuits

## 1. Topology Search

Given the choice of NMOS or PMOS input stage, and the five different op-amp topologies that weâĂŹve talked about (single-stage 5T diff pair with mirror load, single-stage current mirror, two-stage, telescopic cascode, folded cascode), which combinations are appropriate for the following applications? Assume that the magnitude of the N and P threshold voltages is roughly $\pm 0.6 \mathrm{~V}$, and that all overdrive voltages are roughly 0.1 V .
(a) bandgap reference as in GLHM Figure 4.46c driving a $100 \mathrm{k} \Omega$ load

Solution:
All structures could drive a $100 \mathrm{k} \Omega$ load, as load resistance will not affect the DC gain too much.
In the bandgap, the input commom-mode voltage is about 0.7 V and the output voltage is around 1.2 V .
NMOS input is the easiest choice. While a PMOS input might just work, the input common mode needed is close to the edge with $V_{D D}=1.6 \mathrm{~V}$.
With 0.1 V over-drive voltage, all architectures could generate 1.2 V output voltage (assume the cascode use high-swing current mirror load).

- Single-stage 5T diff pair with mirror load NMOS + PMOS
- Single-stage current mirror NMOS + PMOS
- Two-stage NMOS + PMOS
- Telescopic cascode NMOS + PMOS
- Folded-cascode NMOS + PMOS

Rubric: (10 Points)

- +1 : Per correct topology choice
- -1 : Per incorrect inclusion
(b) digital voltage regulator with an output of 1 V and a supply of between 1.6 V and 3.2 V . Consider the scenarios with a load NMOS or PMOS device separately.


## Solution:

For this LDO, with NMOS load, the minimum supply voltage is $1 V+2 V_{o v}+V_{t n}=1.8 V$. This will not work with the low-end of the supply range.
With PMOS load, the input commom voltage is 1 V , and the output voltage is $V d d-V_{o v}-V_{t h p}=$ $V d d-0.7 V$. The PMOS input architectures would not work.

## PMOS load:

- Single-stage 5T diff pair with mirror load NMOS
- Single-stage 5T current mirror NMOS
- Two-stage NMOS
- Telescopic cascode NMOS
- Folded-cascode NMOS

Rubric: (5 Points)

- +1 : Per correct topology choice
- -1 : Per incorrect inclusion
(c) analog voltage regulator with an output of 1.3 V and a supply of between 1.6 V and 3.2 V .


## Solution:

Similar as before, only NMOS input architectures work.

## PMOS load:

- Single-stage 5T diff pair with mirror load NMOS
- Single-stage 5T current mirror NMOS
- Two-stage NMOS
- Telescopic cascode NMOS (just work)
- Folded-cascode NMOS

Rubric: (5 Points)

- +1 : Per correct topology choice
- -1 : Per incorrect inclusion
(d) ADC comparator with an input at 1.25 V and a supply at 1.25 V .


## Solution:

Must use an NMOS input folded cascode, as those are the only ones where the input common mode includes the top rail.

- Folded cascode NMOS

Rubric: (1 Points)

- +1 : Per correct topology choice
- -1 : Per incorrect inclusion
(e) variable gain amplifier with an input at 0 V and a supply at 1.25 V .

Solution:
Must use a PMOS input amplifier to include the bottom rail in the input common mode range.

- Folded cascode PMOS

Rubric: (1 Points)

- +1 : Per correct topology choice
- -1 : Per incorrect inclusion


## 2. Telescopic

Design a telescopic cascode op-amp with a 2V supply, 200 uA tail current and overdrive voltages of roughly 100 mV . Assume the simplest biasing as discussed in class (3 stacked current mirrors). Use the results of your Lab 4 device characterization, and low Vt devices with 1 um channel lengths.
(a) Draw a schematic, showing device sizes and currents, and node bias points.

## Solution:



From Lab4/Lab5 simulation, we get (you might get different numbers, and it's totally fine)

|  | Vth | $\lambda @ L=1 \mu m$ | $\mu C_{o x}$ |
| :---: | :---: | :---: | :---: |
| ne | 0.65 V | $0.141 / \mathrm{V}$ | $140 \mu A / V^{2}$ |
| nel | 0.35 V | $0.161 / \mathrm{V}$ | $150 \mu A / V^{2}$ |
| pe | 0.65 V | $0.091 / \mathrm{V}$ | $30 \mu A / V^{2}$ |
| pel | 0.30 V | $0.151 / \mathrm{V}$ | $60 \mu A / V^{2}$ |

For M1 to M4, $\frac{W}{L}=\frac{I_{t a i}}{\mu C_{o x} V_{o v}^{2}}$
For $\mathrm{Mb}, \frac{W}{L}=\frac{2_{\text {tail }}}{\mu C_{o x} V_{o o}^{o_{o}}}$

|  | $\frac{W}{L}\left(\frac{\mu m}{\mu m}\right)$ |
| :---: | :---: |
| M1A/B | $133 / 1$ |
| M2A/B | $133 / 1$ |
| M3A/B | $333 / 1$ |
| M4A/B | $333 / 1$ |
| Mb | 26771 |

(b) Make a table with device gm and ro

Solution: For M1 to M4, $g_{m}=\frac{I_{\text {Iail }}}{V_{o v}}, r_{o}=\frac{2}{\lambda l_{t} \text { ail }}$
For $\mathrm{Mb}, g_{m}=\frac{2 I_{\text {ail }}}{V_{o v}}, r_{o}=\frac{1}{\lambda I_{t} \text { ail }}$

| Device | $g_{m}$ <br> $(\mathrm{mS})$ | $r_{o}$ <br> $(\Omega)$ |
| :---: | :---: | :---: |
| $\mathrm{M} 1 \mathrm{~A} / \mathrm{B}$ | 2 | 63 K |
| $\mathrm{M} 2 \mathrm{~A} / \mathrm{B}$ | 2 | 63 K |
| $\mathrm{M} 3 \mathrm{~A} / \mathrm{B}$ | 2 | 66 K |
| $\mathrm{M} 4 \mathrm{~A} / \mathrm{B}$ | 2 | 66 K |
| Mb | 4 | 31 K |

(c) Estimate the output impedance, transconductance, and gain of the op-amp

## Solution:

$$
\begin{aligned}
& R_{\text {out }}=\left(r_{o 3}+r_{o 4}+g_{m 3} r_{o 3} r_{o 4}\right)\left\|\left(r_{o 1}+r_{o 2}+g_{m 2} r_{o 1} r_{o 2}\right) \approx g_{m 3} r_{o 3} r_{o 4}\right\| g_{m 2} r_{o 1} r_{o 2} \approx 4 \mathrm{M} \Omega \\
& G_{m}=g_{m 1}=2 m S \\
& \text { Gain }=G_{m} R_{\text {out }}=8 \mathrm{k} \frac{V}{V}
\end{aligned}
$$

(d) Plot the output swing vs. common mode input range (box plot from previous homework)

Solution: To keep all transistor in saturation, input common mode
$V_{c m, \text { min }}=2 V_{o v}+V_{t n}=0.55 \mathrm{~V}$
$V_{c m, \max }=0.75+V_{t n}=1.1 \mathrm{~V}$
and output range is
$V_{\text {out }, \text { min }}=1.2-V_{\text {tn }}=0.85 \mathrm{~V}$
$V_{\text {out }, \text { max }}=1.2+V_{t p}=1.5 \mathrm{~V}$

(e) Could you have made this topology with regular Vt devices?

Solution:

With regular Vt devices, minimum Vdd is
$V d d_{\text {min }}=3 V_{o v}+V_{t n, \text { regular }}+2 V_{o v}+2 V_{t p, \text { regular }}=2.45 \mathrm{~V}>2 \mathrm{~V}$
We cannot use regular Vt devices design this amplifier.

## 3. Telescopic with high-swing current mirror

Repeat the previous problem but with a high-swing current mirror and input-tracking NMOS cascode biasing. Compare the gains. Why are they different?
(a) Draw a schematic, showing device sizes and currents, and node bias points.

Solution:


Use the MOS parameters from Q2. Usually, we want to make the current going to input-tracking NMOS cascode biasing being very small. Here, we neglect the current going to the cascode biasing branch.
For M1 to M4, $\frac{W}{L}=\frac{I_{\text {tai }}}{\mu C_{o x} V_{o v}^{2}}$
For $\mathrm{Mb}, \frac{W}{L}=\frac{L_{\text {lail }}}{\mu C_{o x} V_{o v}^{2}}$

|  | $\frac{W}{L}\left(\frac{\mu m}{\mu m}\right)$ |
| :---: | :---: |
| M1A/B | $133 / 1$ |
| M2A/B | $133 / 1$ |
| M3A/B | $333 / 1$ |
| M4A/B | $333 / 1$ |
| Mb | $267 / 1$ |

$\square$
(b) Make a table with device gm and ro

Solution: For M1 to M4, $g_{m}=\frac{I_{t a i l}}{V_{o v}}, r_{o}=\frac{2}{\lambda I_{t} a i l}$
For $\mathrm{Mb}, g_{m}=\frac{2 I_{\text {tail }}}{V_{o v}}, r_{o}=\frac{1}{\lambda I_{t} \text { ail }}$

| Device | $g_{m}$ <br> $(\mathrm{mS})$ | $r_{o}$ <br> $(\Omega)$ |
| :---: | :---: | :---: |
| $\mathrm{M} 1 \mathrm{~A} / \mathrm{B}$ | 2 | 63 K |
| $\mathrm{M} 2 \mathrm{~A} / \mathrm{B}$ | 2 | 63 K |
| $\mathrm{M} 3 \mathrm{~A} / \mathrm{B}$ | 2 | 66 K |
| $\mathrm{M} 4 \mathrm{~A} / \mathrm{B}$ | 2 | 66 K |
| Mb | 4 | 31 K |

(c) Estimate the output impedance, transconductance, and gain of the op-amp Solution:

$$
\begin{aligned}
& R_{\text {out }}=\left(r_{o 3}+r_{o 4}+g_{m 3} r_{o 3} r_{o 4}\right)\left\|\left(r_{o 1}+r_{o 2}+g_{m 2} r_{o 1} r_{o 2}\right) \approx g_{m 3} r_{o 3} r_{o 4}\right\| g_{m 2} r_{o 1} r_{o 2} \approx 4 \mathrm{M} \Omega \\
& G_{m}=g_{m 1}=2 m S \\
& \text { Gain }=G_{m} R_{\text {out }}=8 \mathrm{k} \frac{V}{V}
\end{aligned}
$$

Wait, actually, $\lambda$ will be different under different Vds's. When $V_{d s}$ drop to $V_{o v}, \lambda$ will increase and the gain will drop.
(d) Plot the output swing vs. common mode input range (box plot from previous homework)

## Solution:

To keep all transistor in saturation, input common mode
$V_{c m, \text { min }}=2 \mathrm{Vov}+V_{t n}=0.55 \mathrm{~V}$
$V_{c m, \max }=1.6+V_{\text {tn }}-V_{o v}=1.85 \mathrm{~V}$
and output range is
$V_{o u t, \max }=V d d-2 V_{o v}=1.8 \mathrm{~V}$
$V_{o u t, \text { min }}=V_{c m}+V_{o v}-V_{t n}=V_{c m}-0.25 \mathrm{~V}$

(e) Could you have made this topology with regular Vt devices? Solution:

With regular Vt devices, minimum Vdd is
$V d d_{\text {min }}=3 V_{o v, n}+V_{o v, p}+V_{t p, \text { regular }}=1.05 \mathrm{~V}<2 \mathrm{~V}$
We can use regular Vt devices in this amplifier.
(f) Compare the gains. Why are they different? Solution:

With larger $\lambda$, the gain and output resistance are smaller than previous circuit, but the output swing and input common-mode volage range become larger.
This is a trade-off between gain and input commom-mode range as well as output swing.

## 4. Telescopic with high-swing current mirror, regular vt devices.

Repeat the previous problem, but with regular Vt devices.
(a) Draw a schematic, showing device sizes and currents, and node bias points.

## Solution:



Use the same table as previous question, but regular devices.
For M1 to M4, $\frac{W}{L}=\frac{I_{t a i}}{\mu C_{o x} V_{o v}^{2}}$
For $\mathrm{Mb}, \frac{W}{L}=\frac{2_{\text {tail }}}{\mu C_{o x} V_{o v}^{\partial o}}$

|  | $\frac{W}{L}\left(\frac{\mu m}{\mu m}\right)$ <br> M1A/B <br> $143 / 1$ |
| :---: | :---: |
| M2A/B | $143 / 1$ |
| M3A/B | $667 / 1$ |
| M4A/B | $667 / 1$ |
| Mb | $286 / 1$ |

(b) Make a table with device gm and ro

Solution: For M1 to M4, $g_{m}=\frac{I_{\text {tail }}}{V_{o o}}, r_{o}=\frac{2}{\lambda_{t} \text { ail }}$
For $\mathrm{Mb}, g_{m}=\frac{2 I_{a i l}}{V_{o v}}, r_{o}=\frac{1}{\lambda I_{t} \text { ail }}$

| Device | $g_{m}$ <br> $(\mathrm{mS})$ | $r_{o}$ <br> $(\Omega)$ |
| :---: | :---: | :---: |
| $\mathrm{M} 1 \mathrm{~A} / \mathrm{B}$ | 2 | 71 K |
| $\mathrm{M} 2 \mathrm{~A} / \mathrm{B}$ | 2 | 71 K |
| $\mathrm{M} 3 \mathrm{~A} / \mathrm{B}$ | 2 | 110 K |
| $\mathrm{M} 4 \mathrm{~A} / \mathrm{B}$ | 2 | 110 K |
| Mb | 4 | 35 K |

(c) Estimate the output impedance, transconductance, and gain of the op-amp

Solution:

$$
\begin{aligned}
& R_{\text {out }}=\left(r_{o 3}+r_{o 4}+g_{m 3} r_{o 3} r_{o 4}\right)\left\|\left(r_{o 1}+r_{o 2}+g_{m 2} r_{o 1} r_{o 2}\right) \approx g_{m 3} r_{o 3} r_{o 4}\right\| g_{m 2} r_{o 1} r_{o 2} \approx 7 \mathrm{M} \Omega \\
& G_{m}=g_{m 1}=2 m S \\
& \text { Gain }=G_{m} R_{\text {out }}=14 \mathrm{k} \frac{V}{V}
\end{aligned}
$$

(d) Plot the output swing vs. common mode input range (box plot from previous homework)

Solution: To keep all transistor in saturation, input common mode
$V_{c m, \text { min }}=2 V_{o v}+V_{t n}=0.85 \mathrm{~V}$
$V_{c m, \max }=1.25-V_{o v}+V_{t n}=1.8 \mathrm{~V}$
and output range is
$V_{o u t, \max }=V d d-2 V_{o v}=1.8 \mathrm{~V}$
$V_{\text {out }, \text { min }}=V_{c m}+V_{\text {ov }}-V_{\text {tn }}=V_{c m}-0.55 \mathrm{~V}$

(e) Compare the gains. Why are they different? Solution:

Compared with lvt devices, the gain and output resistance are larger than previous circuit, but the output swing becomes smaller. The input common-mode range also becomes smaller.

## 5. PMOS Input Folded Cascode

For the PMOS-input folded cascode op-amp below, assume the quadratic model with the following process specs:

- $\mu_{n} C_{o x}=2 \mu_{p} C_{o x}=200 \frac{\mu \mathrm{~A}}{\mathrm{~V}^{2}}$
- $V_{t n}=-V_{t p}=0.3 \mathrm{~V}$
- $C_{o x}=5 \frac{\mathrm{fF}}{\mu \mathrm{m}^{2}}$
- $\lambda=0.1 \mathrm{~V}^{-1}$
- $V_{D D}=2 \mathrm{~V}$
- $C_{o l}=0.5 \frac{\mathrm{fF}}{\mu \mathrm{m}}$

(a) Calculate and tabulate:
i. the overdrive voltage and current in all devices. For this step you may assume that $\lambda=0$. The simplest order may be Mb1 through Mb6, then M1 through M5.


## Solution:

We'll start with Mb1 and work our way through devices

$$
\begin{aligned}
I_{D, b 1} & =\frac{1}{2} \mu_{n} \frac{W}{L} C_{o x} V_{o v}^{2} \\
100 & =\frac{1}{2} \times 200 \times \frac{100}{1} \times V_{o v}^{2} \\
V_{o v, b 1} & =0.1 \mathrm{~V}
\end{aligned}
$$

Note that Mb5 is $\frac{10}{1}$ —a factor of 10 smaller than the other devices! For the same current, it needs an overdrive $\sqrt{10} \times$ larger than its $\frac{100}{1}$ brethren

| Device | Current | Overdrive |
| :---: | :---: | :---: |
|  | $(\mu \mathrm{A})$ | $(\mathrm{V})$ |
| Mb1 | 100 | 0.1 |
| Mb2 | 100 | 0.1 |
| Mb3 | 100 | 0.1 |
| Mb4 | 100 | 0.1 |
| Mb5 | 100 | 0.32 |
| Mb6 | 200 | 0.1 |
| M1A/B | 100 | 0.1 |
| M2A/B | 200 | 0.1 |
| M3A/B | 100 | 0.1 |
| M4A/B | 100 | 0.1 |
| M5A/B | 100 | 0.1 |

ii. Calculate the bias voltages on all nodes, assuming $V_{\mathrm{in}, \mathrm{CM}}=1 \mathrm{~V}$. Specifically: tail, G2, G3, G5, Gb6, S3B, S4AB, and out.

## Solution:

This one is really a lot of $V_{G S}=V_{t}+V_{o v}$ (for the NMOS—switch signs for PMOS).

| Node | Voltage (V) |
| :---: | :---: |
| tail | 1.4 |
| G2 | 0.4 |
| G3 | 0.62 |
| G5 | 1.6 |
| Gb6 | 1.6 |
| S3B | 0.22 |
| S4A/B | 1.6 |
| out | 1.2 |

iii. the $g_{m}$ and $r_{o}$ parameters for M1 through M5.

## Solution:

Assuming our devices are in saturation,

$$
g_{m}=\frac{2 I_{D}}{V_{o v}} \quad r_{o}=\frac{1}{\lambda I_{D}}
$$

| Device $g_{m}(\mathrm{mS})$ $r_{o}(\mathrm{M} \Omega)$ <br> M1 2 0.1 <br> M2 4 0.05 <br> M3 2 0.1 <br> M4 2 0.1 <br>  M5 2 <br> 0.1   |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |

Rubric: (40 Points)

- +1: Per correct overdrive voltage and current each $(22 \times)$
- +1 : Per correct bias voltage $(8 \times)$
- +1 : Per correct $g_{m}$ and $r_{o}$ each $(10 \times)$
(b) Calculate $G_{m}, R_{o}$, and $A_{v 0}$

Solution:

$$
\begin{aligned}
G_{m} \approx g_{m 1} \quad R_{o} & =R_{o, \text { up }} \| R_{o, \text { down }} \\
& \approx\left(g_{m 4} r_{o 5} r_{o 4}\right) \|\left(g_{m 3} r_{o 3}\left(r_{o 2} \| r_{o 1}\right)\right) \\
& =(20 \mathrm{M} \Omega) \|(6.67 \mathrm{M} \Omega)
\end{aligned}
$$

$$
\left|A_{v 0}\right|=G_{m} R_{o}
$$

$$
\begin{aligned}
& G_{m}=2 \mathrm{mS} \\
& R_{o}=5 \mathrm{M} \Omega
\end{aligned}
$$

$$
\left|A_{\nu 0}\right|=10,000 \frac{\mathrm{~V}}{\mathrm{~V}}
$$

Rubric: (3 Points)

- +1: Per correct answer
(c) Calculate the input common mode range and output swing.

Solution: Calculating the input common mode range:

$$
\begin{aligned}
V_{i C M, \max } & =V_{D D}-V_{o v 5}-V_{S G 1} & V_{i C M, \min } & =V_{S 3}-V_{t} \\
& =1.5 \mathrm{~V} & & =-0.08 \mathrm{~V}
\end{aligned}
$$

Calculating the output swing:

$$
\begin{aligned}
V_{o u t, \max } & =V_{D D}-V_{S G 5}-V_{o v 4} \\
& =1.5 \mathrm{~V}
\end{aligned}
$$

$$
V_{\text {out }, \min }=V_{G 3}-V_{t}
$$

$$
=0.32 \mathrm{~V}
$$

$$
\begin{aligned}
V_{i C M} & \in[-0.08,1.5] \mathrm{V} \\
V_{\text {out }} & \in[0.32,1.5] \mathrm{V}
\end{aligned}
$$

Rubric: (8 Points)

- +1 : Per correct equation $(4 \times)$
- +1 : Per correct numerical answer $(4 \times)$
(d) What is the minimum voltage that could be used on the gates of M3AB to still keep M2AB in saturation? If you used that voltage, what is the new input common mode range and output swing? How would you change the size of Mb5 to achieve that voltage?


## Solution:

$$
\begin{aligned}
V_{G 3, \min } & =V_{o v 2}+V_{G S 3} \\
& =0.5 \mathrm{~V}
\end{aligned}
$$

For the common mode range and swing:

$$
\begin{aligned}
V_{i C M, \max } & =V_{D D}-V_{o v 5}-V_{S G 1} \\
& =1.5 \mathrm{~V} \text { (no change) } \\
V_{o u t, \max } & =V_{D D}-V_{S G 5}-V_{o v 4} \\
& =1.5 \mathrm{~V} \text { (no change) }
\end{aligned}
$$

$$
\begin{aligned}
V_{i C M, \min } & =V_{S 3}-V_{t} \\
& =V_{G 3}-V_{G S 3}-V_{t} \\
& =-0.2 \mathrm{~V} \\
V_{\text {out }, \min } & =V_{G 3}-V_{t} \\
& =0.2 \mathrm{~V}
\end{aligned}
$$

And finally to change the sizing of Mb5 to get that voltage:

$$
\begin{aligned}
V_{o v b 5} & =V_{G 3}-V_{t} \\
& =0.2 \mathrm{~V} \\
I_{D b 5} & =\frac{1}{2} \mu_{n} C_{o x} \frac{W}{L} V_{o v b 5}^{2} \\
\frac{W}{L} & =\frac{2 I_{D b 5}}{\mu_{n} C_{o x} V_{o v b 5}^{2}} \\
& =25
\end{aligned}
$$

which makes sense since to sink the same current with twice the overdrive requires a size down of $4 \times$ relative to the larger device.

$$
\begin{gathered}
V_{G 3, \min }=0.5 \mathrm{~V} \\
V_{i C M} \in[-0.2,1.5] \mathrm{V} \\
V_{\text {out }} \in[0.2,1.5 \mathrm{~V}] \mathrm{V} \\
\quad\left(\frac{W}{L}\right)_{b 5}=\frac{25}{1}
\end{gathered}
$$

Rubric: (7 Points)

- +1 : Correct method for $V_{G 3, \text { min }}$
- +1 : Correct numerical value for $V_{G 3, \min }$
- +1: Per correct boundary of input common mode and output swing given $V_{G 3}(4 \times)$
- +1 : Correct change in sizing
(e) If the load capacitance is roughly 1 pF (roughly the same as the input capacitance),
i. what are the pole and unity gain frequencies?


## Solution:

We have a dominant pole

$$
\begin{aligned}
\omega_{p} & =\frac{1}{R_{o} C_{L}} \\
& =\frac{1}{5 \mathrm{M} \Omega \times 1 \mathrm{pF}} \\
& =0.2 \times 10^{6} \frac{\mathrm{rad}}{\mathrm{~s}} \\
\omega_{u} & =\frac{G_{m}}{C_{L}} \\
& =\frac{2 \mathrm{mS}}{1 \mathrm{pF}} \\
& =2,000 \times 10^{6} \frac{\mathrm{rad}}{\mathrm{~s}}
\end{aligned}
$$

$$
\begin{aligned}
\omega_{p} & =0.2 \times 10^{6} \frac{\mathrm{rad}}{\mathrm{~s}} \\
\omega_{u} & =2,000 \times 10^{6} \frac{\mathrm{rad}}{\mathrm{~s}}
\end{aligned}
$$

Rubric: (2 Points)

- +1: Correct $\omega_{p}$
- +1 : Correct $\omega_{u}$
ii. what is the phase margin in unity gain?


## Solution:

To calculate the phase margin we should first calculate non-dominant poles and zeros. The two diode connections give 2 poles and a zero while the cascode contributes one non-dominant pole. The respective values are as shown:

$$
\begin{aligned}
\omega_{p, \text { cascode }} & =\frac{g_{m 3}}{C_{g s, 3}} \\
& =\frac{g_{m 3}}{\frac{2}{3} W_{3} L_{3} C_{o x}+W_{3} C_{o l}^{\prime}} \\
& =\frac{2,000 \mu \mathrm{~S}}{\frac{2}{3} \times 100 \times 1 \times 5 \mathrm{fF}+100 \times 0.5 \mathrm{fF}} \\
& =5.22 \times 10^{9} \frac{\mathrm{rad}}{\mathrm{~s}}
\end{aligned}
$$

$$
\begin{aligned}
\omega_{p, \text { mirror } 1,2} & =\frac{g_{m 5}}{2 C_{g s, 5}} \\
& =1.3 \times 10^{9} \frac{\mathrm{rad}}{\mathrm{~s}} \\
\omega_{z, \text { mirror }} & =\frac{g_{m 5}}{\sqrt{2} C_{g s, 5}} \\
& =1.84 \times 10^{9} \frac{\mathrm{rad}}{\mathrm{~s}}
\end{aligned}
$$

Calculating the phase margin can be found as

$$
\begin{aligned}
\phi_{\mathrm{PM}} & =180-\tan ^{-1}\left(\frac{\omega_{u}}{\omega_{p}}\right)-2 \tan ^{-1}\left(\frac{\omega_{u}}{\omega_{p, \text { mirror }}}\right)+\tan ^{-1}\left(\frac{\omega_{u}}{\omega_{z, \text { mirror }}}\right)-\tan ^{-1}\left(\frac{\omega_{u}}{\omega_{p, \text { cascode }}}\right) \\
& \approx-8^{\circ}
\end{aligned}
$$

using the small angle approximation.

$$
\phi_{\mathrm{PM}} \approx-8^{\circ}
$$

Rubric: (7 Points)

- +1 : Per correct method for calculating a non-dominant pole or zero $(4 \times)$
- +5 : Correct method for calculating phase margin
- +1 : Correct numerical value of phase margin
iii. what are the frequencies of the pole/zero doublets from the current mirror?


## Solution:

See above.
Rubric: (2 Points)

- +1 : Per correct answer
(f) (EE240A) How does the performance for the amplifier above change
i. if the bias current drops to $1 \mu \mathrm{~A}$ and all devices are biased at roughly $V_{g s}=V_{t}$ ?

Rubric: (4 Points)

- +2 : Estimated change in gain
- +2: Estimated change in bandwidth, phase margin
ii. if the bias current remains $100 \mu \mathrm{~A}$, but the length of all devices is changed to 14 nm , and the widths vary from 200 nm to 400 nm as appropriate for a current density of $0.5 \frac{\mathrm{~mA}}{\mu \mathrm{~m}}$ ? Assume that the load capacitance is comparable to the input capacitance (which is...?).
Rubric: (4 Points)
- +2 : Estimated change in gain
- +2 : Estimated change in bandwidth, phase margin


## 6. Continuing...

To increase the positive output swing of the previous amplifier,
(a) redraw the PMOS current mirror $\mathrm{M} 4 \mathrm{AB}, \mathrm{M} 5 \mathrm{AB}$ as a high-swing cascode current mirror, as in Figure 5.18 b in Razavi ( $5.13 b$ in the 1 st edition), but PMOS.

## Solution:



This presents a couple of issues:

- What is the "right" value of $V_{B P}$ (especially across supply and temperature)
- How to generate $V_{B P}$ ?

Rubric: (1 Points)

- +1 : Correctly redrew the figure as PMOS
(b) Generate $V_{b}\left(V_{G 4}\right)$ using something like Mb5 above, but PMOS. What current source do you use? What gate voltage biases it? What $\left(\frac{W}{L}\right)$ do you use for all devices, and why?
Solution: There are a few different ways to achieve this. The first way is generating $V_{B P}$ independent of the actual mirror with something like so:


$$
\begin{aligned}
V_{B P} & =V_{D D}-V_{S G, \mathrm{Mb}} \\
& =V_{D D}-\left(\sqrt{\frac{2 I_{D}}{\mu_{p} C_{o x} \frac{W}{L}}}+V_{t p}\right) \\
& =V_{D D}-\left(2 V_{o v}+V_{t}\right)
\end{aligned}
$$

$$
\left(\frac{W}{L}\right)_{\mathrm{Mb}}=\frac{1}{4} \times\left(\frac{W}{L}\right)_{4}
$$

Alternatively, you can resort to what's known as the self-biased mirror:

where

$$
\begin{aligned}
V_{\mathrm{bot}} & =V_{S G 4 B}+V_{o v} \\
& =V_{\mathrm{top}}+I_{\mathrm{REF}} R_{b}
\end{aligned}
$$

To have the same $I_{\text {REF }}=I_{\mathrm{O}}, \mathrm{M} 4 \mathrm{~A}=\mathrm{M} 4 \mathrm{~B}=\mathrm{M} 5 \mathrm{~A}=\mathrm{M} 5 \mathrm{~B}$, so

$$
V_{S G 4 B}=V_{S G 5 A}=V_{\mathrm{top}}
$$

and so to remain in saturation,

$$
R_{b} \leq \frac{V_{o v}}{I_{\mathrm{REF}}}
$$

Rubric: (4 Points)

- +1 : Some viable circuit
- +3: Indication of restrictinos associated with the biasing circuit (e.g. current sources, gate voltage, device sizing)
(c) (EE240A) Generate $V_{b}$ from the circuit suggested in 5.19 b in Razavi. What value for $\left(\frac{W}{L}\right)_{5}$ in that figure is needed?
Solution:
For reference, the topology:


We know $V_{\text {OUT }}=1.2 \mathrm{~V}$, meaning $V_{\text {ov } 5}=0.5 \mathrm{~V}$. To sink the same amount of current as in the previous subparts, we consider the ratio of the new $V_{o v}$ and the old one. If it increases by a factor of 5, the size needs to decrease by a factor of 25 to sink the same amount of current as before, so

$$
\left(\frac{W}{L}\right)_{5}=\frac{8}{1}
$$

Rubric: (2 Points)

- +2: Correctly solved for $\left(\frac{W}{L}\right)_{5}$


## 7. Regulator Feedback

In Figure 2 of this Analog Devices discussion on voltage regulators: https://www.analog.com/en/ design-center/landing-pages/001/fundamentals-of-ldo-design-and-applications. html
(a) Estimate the low-frequency loop gain $T$ in terms of the op-amp voltage gain $A_{\nu 0}, g_{m}$ of the pass transistor, and load resistance $R_{L}$ (not shown in the figure).
Solution:


Figure 2. ADP1740 internal block diagram.


To find $T$, we need to break the loop at a point where all feedback loops are broken and find the gain from one side of the break back around to the other side of the break.


In the diagram above, we've broken the loop and we need to find the voltage gain from $V_{+}$to the other side of the loop break.

$$
T=A_{v 0} g_{m}\left(r_{o}\left\|R_{L}\right\|\left(R_{1}+R_{2}\right)\right) \times \frac{R_{2}}{R_{1}+R_{2}}
$$

Rubric: (5 Points)

- +1: Broke loop at a point which actually broke the feedback loop
- +2: Correct method (and direction) for calculating loop gain
- +2: Correct final answer
(b) Why does the SENSE value connect to the positive input of the op-amp? Is this positive feedback?

Solution:

This is not positive feedback! The reason it's connected to the positive input of the op amp is because the MOSFET at the output of the op amp introduces an inversion in the feedback loop.

Rubric: (1 Points)

- +1: Correct answer and explanation


## 8. Programmable Gain Amplifier

For the circuit in figure 13.43 in Razavi (6.9 in GHLM)
(a) What ratios of $C_{2}$ to $C_{1}$ are needed to make a variable gain amplifier with gain equal to any integer between 1 and 8 ?

## Solution:

In the first phase, we calculate the (positive) charge at the negative input of the amplifier.

$$
Q_{X}=C_{1}\left(-V_{i n}\right)
$$

In the second phase, we calculate the charge on the same node

$$
Q_{X}=C_{2}\left(-V_{\text {out }}\right)
$$

And since charge is conserved,

$$
\frac{V_{\text {out }}}{V_{\text {in }}}=\frac{C_{1}}{C_{2}}
$$

If $C_{2}=C_{0}$, we need $C_{1}$ to fall in $\left\{C_{0}, 2 C_{0}, \ldots, 8 C_{0}\right\}$.

Rubric: (2 Points)

- +1 : Correct expression of voltage gain
- +1 : Correct answer of ratios
(b) For a given open-loop op-amp gain $A$, which of the closed-loop gains above has the worst gain error? (you may assume that $C_{P}=0$ )


## Solution:

The gain error is given by $\varepsilon_{\text {gain }}=-\frac{1}{A_{0} f}$ where the feedback factor $f$ is related to $A_{v}$ by $f=\frac{1}{A_{v}}-\frac{1}{A_{0}}$. Thus, $\varepsilon_{\text {gain }}$ has the largest magnitude when $f$ is smallest, which happens when $A_{v}=8$.

The highest closed loop gain $A_{v}=8 \mathrm{~V} / \mathrm{V}$

Rubric: (2 Points)

- +1 : Correct method for calculating gain error
- +1: Correct answer
(c) If the desired closed-loop gain accuracy is $0.4 \%$ regardless of gain setting, what is the minimum openloop gain necessary for the op-amp?
Solution: Looking to the worst case, we can solve

$$
\begin{aligned}
\frac{1}{A_{0} f} & \leq 0.004 \\
\frac{1}{\frac{A_{0}}{A_{v}}-1} & \leq 0.004 \\
A_{0} & \geq A_{v}\left(\frac{1}{0.004}+1\right) \\
& =2008
\end{aligned}
$$

$$
A_{0} \geq 2008 \mathrm{~V} / \mathrm{V}
$$

Rubric: (2 Points)

- +1 : Correct equation for loop gain
- +1 : Correct numerical answer given your answer about the highest closed loop gain
(d) If the amplifier must settle to within $0.4 \%$ of the correct value within $10 \mu \mathrm{~s}$, what is the minimum unity gain bandwidth of the op-amp?


## Solution:

For fractional settling error of a single-pole system, we have

$$
\varepsilon_{\text {settle }}=e^{-\frac{t}{\tau}}
$$

So for a settling time $t_{s}=10 \mu \mathrm{~s}$ and an error $\varepsilon_{\text {settle }}=0.004$, we can solve for $\tau$

$$
\begin{aligned}
\tau & =\frac{t_{s}}{\ln \left(\frac{1}{\varepsilon_{\text {setlle }}}\right)} \\
& \approx 1.8 \mu \mathrm{~s}
\end{aligned}
$$

Here we assume a single-pole system where the unity gain bandwidth is the gain-bandwidth product

$$
\begin{aligned}
\omega_{u} & =A_{v 0} \times \frac{1}{\tau} \\
& \approx 4.4 \frac{\mathrm{Mrad}}{\mathrm{~s}}
\end{aligned}
$$

$$
\omega_{u} \geq 4.4 \frac{\mathrm{Mrad}}{\mathrm{~s}}
$$

Rubric: (2 Points)

- +1 : Correct method
- +1: Correct final numerical answer


## 9. More Folded Cascode (EE240A)

For the folded cascode above, how does performance change
(a) if the bias current drops to $1 \mu \mathrm{~A}$ and all devices are biased at roughly $V_{G S}=V_{t}$ ?

Rubric: (4 Points)

- +1: Gain should increase
- +1: Quantitative analysis of how gain increases
- +1: Bandwidth should decrease
- +1: Quantitative analysis of how bandwidth should decrease
(b) if the bias current remains at $100 \mu \mathrm{~A}$, but the length of all devices is changed to 14 nm , and the widths vary from 200 nm to 400 nm as appropriate for a current density of $0.5 \mathrm{~mA} / \mu \mathrm{m}$ ? Assume the load capacitance is comparable to the input capacitance (which is?).
Rubric: (6 Points)
- +2: Estimated input capacitance
- +2: Description of how gain will change with reasonable explanation
- +2: Description of how bandwidth will increase with reasonable explanation

