# EE 140/240A Linear Integrated Circuits
# Fall 2019 Lab 4

## Introduction

For this lab, you may consult the professor, the TAs, your friends, the textbook, the internet, and any other living or inanimate objects, with the exception of your peers' lab reports. You may obtain data in pairs, but must **submit your own written report**. Be concise. Hand calculations should be to 1 or at most 2 digits of precision.

## Objective: Process Characterization and PVT-Insensitive Biasing

For each problem you will be exploring the models of several different devices: short channel and long channel, NMOS and PMOS, and different flavors of devices (low-threshold, regular threshold voltage, and higher voltage tolerance).

| | $\frac{W}{L}$ |
|---|---|
| short channel | $10L_{\min}/L_{\min}$ |
| long channel | 10µm/1µm |

In general you will have four answers to each question, e.g. "PMOS short channels look quadratic over the range…, NMOS long channels look quadratic over the range…," etc. You may find it easiest to plot each device on a different plot.

## Prelab

(1) With $|V_{ds}| = 1.5$V, use Cadence to simulate $I_d$ vs. $V_{gs}$ for $V_{gs}$ from 0V to $V_{DD} = 1.8$V. Do this for devices `ne`, `nel`, `pe`, and `pel`.

   a. Plot all of the currents. Do the short channel devices look like our velocity saturation model? Do the long channel devices look quadratic? Over what range of $V_{gs}$ for each?

   b. Over the range where the device looks velocity saturated (if any), estimate $C_{ox}v_{scl}$ and $V_t$.

   c. Plot $\sqrt{I_d}$. What is the range of $V_{gs}$ for which the curves look linear? For that range, estimate $\mu C_{ox}$ and $V_t$.

   d. Compare your estimates of $V_t$ for each device from parts 1.b and 1.c.

   e. Plot $\log_{10}(I_d)$. What is the range over which each curve looks straight? Estimate the non-ideality factor $n$ and $\frac{I_s}{W}$ for each subthreshold model in those regions.

   f. Plot $g_m$ for all devices vs. $V_{gs}$. Which device, at what bias point, gives the best $g_m$?

   g. Plot $\frac{g_m}{I_d}$ for all devices vs. $V_{gs}$. How does this compare to theory for sub-threshold, quadratic, and saturation models? Where are the transitions?

   h. Which device, at what bias point, gives the best $g_m$ per µA? This is one of the most important metrics of performance.

(2) For the same devices as above, simulate $I_{ds}$ vs. $V_{ds}$ from $V_{ds}$ from 0V to $V_{DD} = 1.8$V with $|V_{gs}| = 1.0$V.

   a. Plot $I_{ds}$ and $r_o$ on the same plot.
   b. Is there a clear transition to saturation for each device? Does it happen where you expect, relative to the $V_t$ values calculated above?
   c. Try to pick the best value for $\lambda$ that you can, and sketch by hand what you expect. Is $r_o = \frac{1+\lambda V_{ds}}{\lambda I_d}$ a good model for output resistance for any/some/all of these devices?
   d. Which device, at what bias point, gives the highest intrinsic gain?

(3) Now for the devices `ne5` and `pe5`, tabulate the following

- Over what $V_{GS}$ region the devices look quadratic or velocity saturated in the same fashion as 1.a
- $C_{ox}v_{scl}$ for devices when they're velocity saturated
- $V_t$
- $\mu C_{ox}$
- The nonideality factor $n$ and $I_S/W$
- A plot of $g_m/I_D$
- $\lambda$

with the new parameters:

| Parameter | Value |
|---|---|
| $V_{DD}$ | 5V |
| $V_{DS}$ | 4.5V |
| $\left(\frac{W}{L}\right)_{\text{short}}$ | $\frac{5\mu\text{m}}{500\text{nm}}$ |
| $\left(\frac{W}{L}\right)_{\text{long}}$ | $\frac{50\mu\text{m}}{5\mu\text{m}}$ |

(a) $I_D$ vs. $V_{GS}$ parameters

| Parameter | Value |
|---|---|
| $V_{DD}$ | 5V |
| $V_{GS}$ | 1.5V |
| $\left(\frac{W}{L}\right)_{\text{short}}$ | $\frac{5\mu\text{m}}{500\text{nm}}$ |
| $\left(\frac{W}{L}\right)_{\text{long}}$ | $\frac{50\mu\text{m}}{5\mu\text{m}}$ |

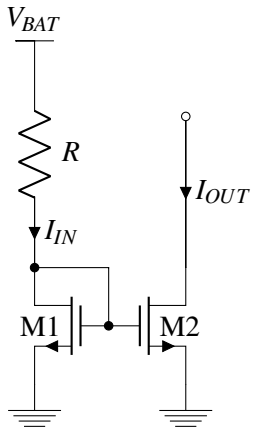
(b) $I_D$ vs. $V_{DS}$ parameters

(4) Estimate $C_{gs}$ for each device. Estimate the unity gain frequency for each device in a common source amplifier with an ideal current source load when driving a copy of itself.

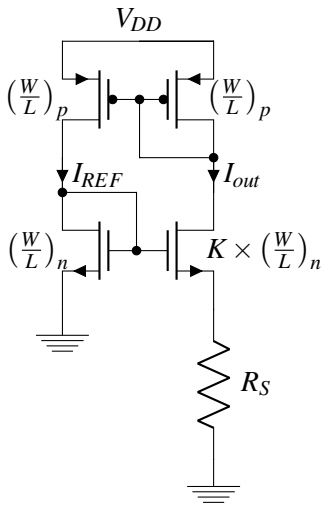
# Lab

**For the design portions of the lab, you may use any flavor of NMOS or PMOS device available within the PDK, though you will be responsible for characterizing them if you choose devices other than those mentioned in the prelab.**

The simple resistor-biased current mirror is included as a control to see how bad things can be. The constant-$g_m$ source is a step in the right direction, and is good enough for some applications.




(a) Resistively biased current mirror




(b) The "constant $g_m$" reference circuit

- Design both circuits to have a nominal output current $I_{OUT} = 10\mu A$. For the current mirror, tie the output node to a voltage source $V_{OUT} = V_{BAT}/2$ (see the next bullet point)
- Plot the output current and gate bias voltage on the NMOS devices in both circuits vs. temperature and battery voltage. For the battery voltage, you have access to two alkaline cell batteries. If you choose to use two batteries, your battery voltage will go from 1.6V to 3.2V. Note that some devices are rated for 1.8V! **Extra Credit**: Work with one alkaline battery where the $V_{BAT}$ will go from 0.8V to 1.6V.
- Tabulate the worst-case variation.

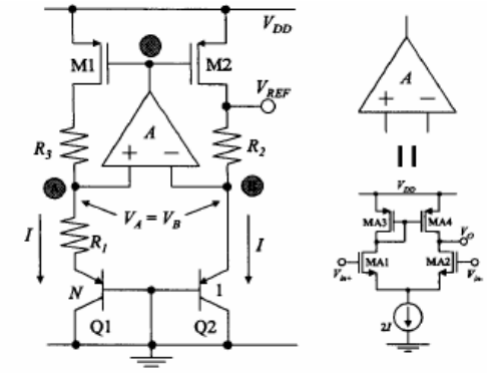



Figure 2: Mok, Philip KT, and Leung, Ka Nang. "Design Considerations of Recent Advanced Low-Voltage Low-Temperature-Coefficient CMOS Bandgap Voltage Reference." Custom Integrated Circuits Conference, 2004. http://web.mit.edu/Magic/Public/papers/IEEEXplore(14).pdf

Now you will design the bandgap circuit shown above to generate $V_{REF} = 1.2$V. Once again, you may choose $V_{BAT} \in [0.8, 1.6]$ V or $[1.6, 3.2]$ V.

- We'll set $R_3 = R_2$.

- Your op amp may be a simple differential pair or a two-stage op amp. It needs to run off of $V_{BAT}$ because at this point you don't have any other voltages to work from.
- The bipolar PNP transistors are actually diodes. Use any diode or bipolar element you please from the xt018 toolkit. Make Q1 and Q2 the same dimensions and then use the "multiplier" field to put copies of each in parallel. The ratio of the size of Q1 to Q2 should be a rational number.
- The resistors should have a temperature coefficient. You can start with analogLib resistors, but you must replace them with your choice of resistor (except pfuse) from the xt018 toolkit.
- **[Writeup]** Show that the current in both branches is

$$I = \frac{\Delta V_{BE}}{R_1}$$

- **[Writeup]** Write an expression for $V_{REF}$ in terms of $\Delta V_{BE}$, $V_{BE}$, $R_1$, and $R_2$.
- **[Writeup]** Now rewrite your expression for $V_{REF}$ in terms of $I_s$, $V_{BE}$, $V_t$, $R_1$, $R_2$, and $N$.
- **[Writeup]** Now choose values for $N$ and for the ratio of $\frac{R_2}{R_1}$ to get close to a zero temperature coefficient. Use only rational numbers for $N$ and the ratio. We do this so that we make the resistors and capacitors match very well during layout by constructing them from unit elements.
- Choose a starting size for Q2. We will iterate and adjust this later.
- **[Writeup]** Calculate what $V_{BE2}$ should be in order to generate $V_{REF} = 1.2\text{V}$ given your previous choices.
- **[Writeup]** Simulate a copy of the Q2 diode to find how much current is required to give the value of $V_{BE2}$ you calculated.
- **[Writeup]** Calculate the size of $R_2$ now that you know the current through it and voltages across it.
- **[Writeup]** Calculate the size of $R_1$ using the ratio you picked earlier. Note that we have a tradeoff here between the size of the resistors and the bias current through the diodes. If your resistors are extremely large (many MΩ), you can adjust your diode size and recalculate.
- **[Writeup]** Size the PMOS transistors to deliver the calculated current with an overdrive of a few hundred millivolts.
- Now that you have finished sizing all the components, you can return to your choices made earlier and adjust if necessary.
- Set a value for $V_{BAT}$ and run a DC simulation sweeping the temperature from $-40°\text{C}$ to $+85°\text{C}$. **[Writeup]** Plot $V_{REF}$ (and specify $V_{BAT}$). Ideally the output should look parabolic with a slope of zero near 25°C. You will likely need to make adjustments.
- **[Writeup]** If you need to make adjustments, think about what the slope of your output is telling you. You likely have too much of either the positive temperature coefficient or the negative. Make adjustments to balance these so they add up to zero near 25°C.
- **[Writeup]** Once you have a relatively flat temperature response, rerun the simulation varying $V_{BAT}$ from 0.8V to 1.6V (or 1.6V to 3.2V) in steps of 200mV.

- If you chose to use a single alkaline battery, you likely noticed serious performance hits when $V_{BAT}$ began to drop. While this isn't ideal, using a high battery voltage relative to your $V_{REF}$ (which you'll be using as a reference for voltage regulation later) can potentially waste a lot of power.