

EE 140/240A Linear Integrated Circuits
Fall 2019

Lab 5

Introduction

For this lab, you may consult the professor, the TAs, your friends, the textbook, the internet, and any other living or inanimate objects, with the exception of your peers' lab reports. You may obtain data in pairs, but must **submit your own written report**. Be concise. Hand calculations should be to 1 or at most 2 digits of precision. **Don't use a calculator—I won't let you use one on the exam and it's good to get in practice.**

Objective: Folded Cascode Design

The goal is to design and simulate a PMOS input folded cascode for your Variable Gain Amplifier (VGA). The figures below show the topology circuitry of a PMOS input folded cascode (Does this topology reasonable in our technology? If not, how would you modify it?). You also need to design the bias circuit to bias your amplifier. The const-gm circuit from Lab 4 is good candidate to start with. In any case, you might want to start with longer channel lengths (e.g. $L = 1\mu m$) to keep the devices in quadratic mode where they are easier to analyze. There are many ways to bias this circuit, this is only one of many possibilities.

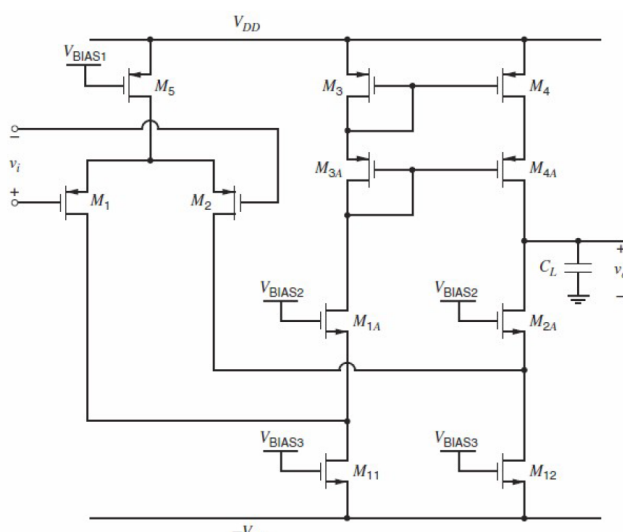


Figure 1: PMOS Input Folded Cascode

Specification	Requirement
V_{DD}	1.2V
Settling Accuracy ($f = \frac{1}{8}$)	$< 0.4\%$
Settling Time ($f = \frac{1}{8}$)	$< 5\mu s$
C_L	400fF
Input Common Mode Range	Includes ground
Temperature	$-40^\circ\text{C} < T < +85^\circ\text{C}$

Recommended Design Strategy

- (1) Calculate the requirements for open loop gain and unity gain bandwidth.
- (2) Choose device lengths ($L = 1\mu\text{m}$ is a good place to start) and overdrive voltages.
- (3) Calculate the transconductance required for the bandwidth and the current given your choice of overdrive voltage.
- (4) Calculate widths for all transistors. Start with the current mirror for the input diff pair and work your way toward the output. The table below should give you a reasonable place to start with hand calculations using the quadratic model.
- (5) After sizing all transistors run a DC sim and check all the voltages and currents (Don't forget to apply a DC bias at the input). If the simulated values are very far off from what your hand calculations predicted, STOP! Go back through systematically and look for the discrepancy. If your DC bias is wrong, your amplifier is never going to work as expected.
- (6) Once your DC bias is working, use the test bench (see below) to check the AC small signal frequency response of your amplifier. If you fail to meet your gain or bandwidth specs, think about what you need to change in order to increase the gain or bandwidth and make those changes. Keep track of what changes you make and what their effects were (making copies of your schematics with revision numbers is recommended). Continue this strategy until you have met all specs.
- (7) You'll likely find that one temperature condition is more difficult to meet than the others. It is easiest to focus on getting your amplifier working under this most difficult constraint, then the other temperatures should achieve the specs with ease.

	Vth	$\lambda @ L = 1\mu m$	μC_{ox}
ne	0.65V	0.14 1/V	$140\mu A/V^2$
nel	0.35V	0.16 1/V	$150\mu A/V^2$
pe	0.65V	0.09 1/V	$30\mu A/V^2$
pel	0.30V	0.15 1/V	$60\mu A/V^2$

TestBench

We often use components from analogLib to test our circuits (things like voltage sources, etc) but we want our schematics to only include real devices that we can fabricate (this becomes important for layout). The solution is to create a test wrapper which turns our schematic with real devices into a component with input and output pins. We can then create a new schematic, instantiate the symbol of our circuit, and

attach analogLib parts to the pins for testing. Since we will use test benches to evaluate your final project performance, you will get familiar with the process in this lab. The test bench has already been created for you as an example. The overview of the steps to use the test bench are outlined below, and then explained in detail:

- (1) Copy over the test bench file, zz_pmos_cascode from library: ee140_gsi
- (2) Copy your schematic to the test bench library
- (3) Load saved state and run simulation

To setup your testbench, you need to follow these steps:

- (1) Copy over the testbench and amplifier symbol from library: ee140_gsi
 - a. In your Library Manager, click Edit → Library Path. The Library Path Editor will pop up. By click on Edit → Add Library, you can add the ee140_gsi library in /home/ff/ee140/fa19/cadence folder.

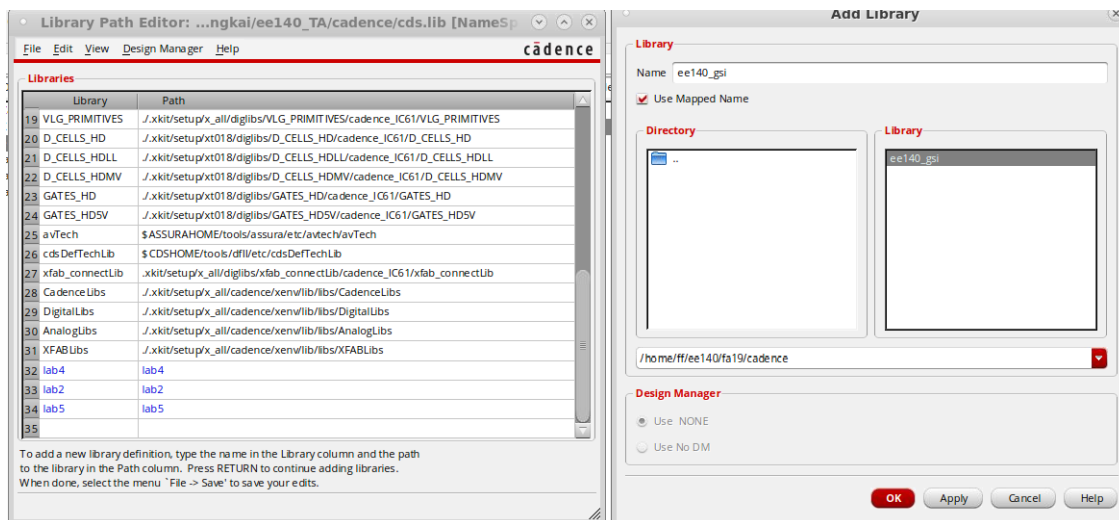


Figure 2: Library Manager

Click OK and save your changes.

- b. Once this is ensured, copy "zz_pmos_cascode" and "pmos_cascode_wrap" by right Click → Copy.
- c. In the pop-up menu make sure to provide your library name under "To". By default it would be "ee140_gsi" which you need to replace it with name of your design library.

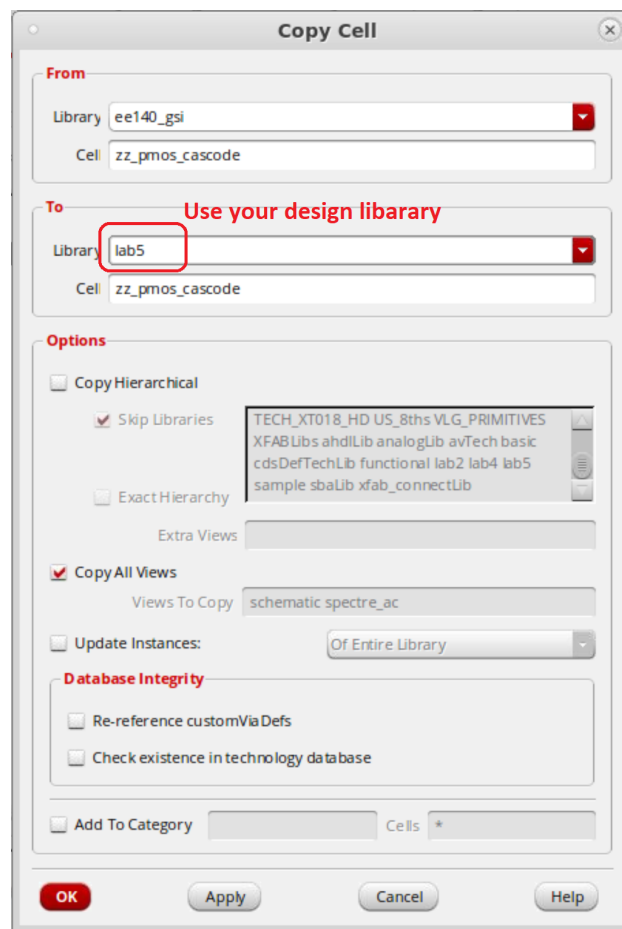


Figure 3: Copy Cell

- d. If you get a window showing the Copy Problems, click on Overwrite All and then click on OK. This would finish copying the cell to your library.

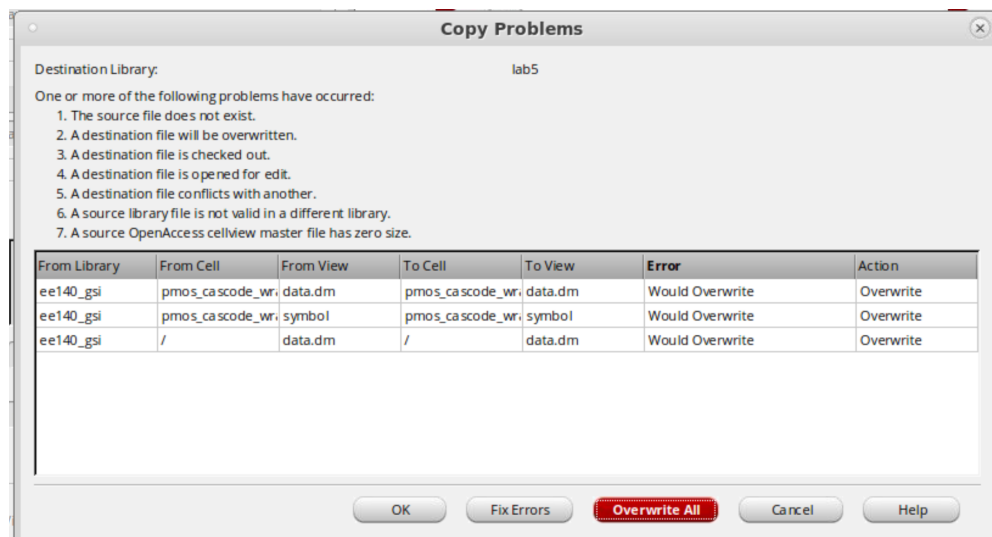


Figure 4: Copy Problems

- e. You need to do exact same steps for both "zz_pmos_cascode" and "pmos_cascode_wrap".
- (2) Copy your schematic to the test bench library.
- Make sure your schematic has the same pin names and types as the pmos_cascode_wrap cell. In the given cell, the two inputs are called "INP" and "INN", with input type. The output is called "OUT" with output type. The supplies are called "VDD" and "VSS", with inputOutput type.
 - Cell pmos_cascode_wrap only contains the symbol only. You should copy your schematic view into this cell by right click on your schematic. Choose copy and fill out the form as below.

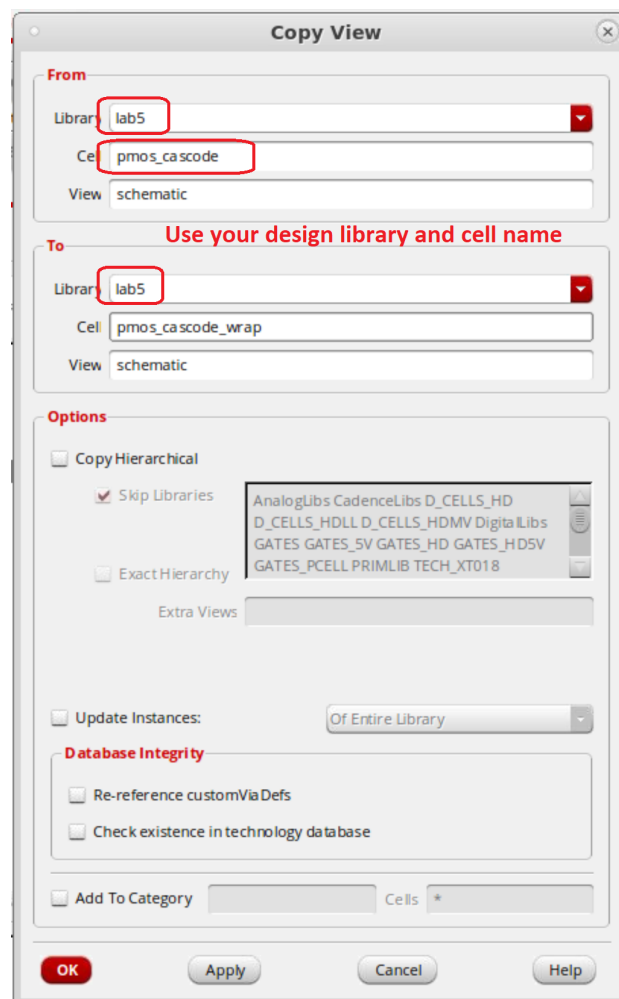


Figure 5: Copy Schematic

- c. Click "OK" in the copy window. If you get warnings about data.dm, they are safe to ignore and overwrite as the previous step.
- (3) Load saved state and run simulation.
- The other cell inside zz_pmos_cascode has two views. One is the test bench schematic which instantiates your amplifier symbol along with analogLib parts for testing. The other is a saved ADE state called "spectre_ac". Saved states allow you to save a particular simulation configuration so that you can easily run it again later.

- b. Double click on "spectre_ac". This will open ADE with DC and AC simulations already set up. There are also variables for VDD and the common mode input voltage which default to 1.2 V and 0 V respectively. Click run. If you have set everything up correctly a plot should open showing the magnitude and phase response.

Debugging

It's a good idea to build things in pieces and test as you go. You could start with the bias network, building up the circuit one leg at a time and verifying that you get the expected gate bias voltages, and then adding in the transistors in the signal path. Or you could build the signal path first, with ideal sources to set biases, and verify that it operates the way that you expect before adding in the bias network. "Test as you go" means "do a hand analysis to estimate bias point voltages and currents, smallsignal model parameters, gain, BW, etc., and then check with simulation to make sure that is what your circuit is doing".

If SPICE and hand analysis don't match, stop! Go back and figure out if your analysis is wrong, or you built the circuit wrong, or what. A DC plot of V_{out} vs. V_+ will tell you gain and output swing (take a derivative and see how close you can get to the rails before the gain drops off). That same plot with several different values for V_- will give you an idea of what your input common mode range is, and how gain and swing vary with input common mode. Estimate phase margin, and then put the amplifier in unity gain feedback and see if the response to a step input looks like you expect.

Deliverables

- (1) Show how you calculated gain and bandwidth requirements.
- (2) Schematic of opamp and bias generation with sizes and currents annotated. (Cadence snapshots are discouraged for the schematic. You can use other softwares to draw your schematic, such as circuitikz, Illustrator, Visio, etc. The Illustrator templates are attached to the website. If you have to use Cadence snapshot, make sure your diagram is legible.)
- (3) Bode plots of amplifier frequency response (mag and phase) under different temperatures. (You should use white background for bode plots with 3dB frequency and DC gain annotated. You can use Cadence screenshots or redraw it with plotting softwares of your choice. Be sure to label your axis!)
- (4) The following table:

Temperature	DC Gain	Unity Gain Bandwidth	Phase Margin
-40°C			
27°C			
85°C			