Project

Wafer sort

probe machine
probe card
laser trim
digital trim - OTP, flash

telescopic cascode

folded cascode

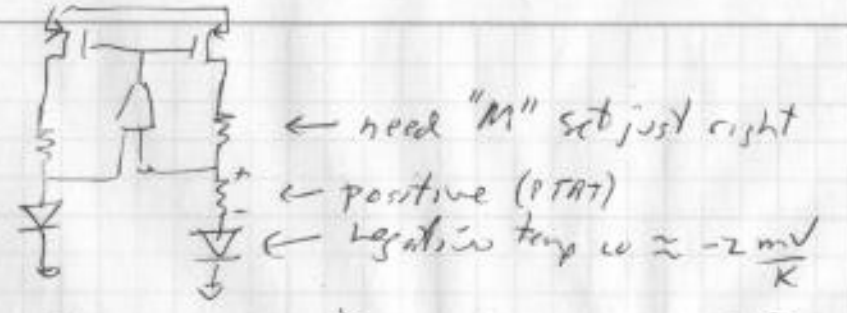
high swing biasing

switched capacitors

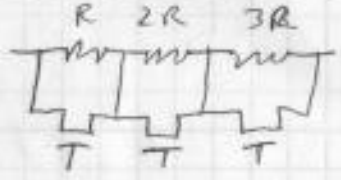
Lab 4

Device modeling

correction from last lecture LVT not ϕVT



one of many clever ways to set BG voltage



how to set R_1?

measure and trim w/ LASER (old)
digitally programmed (today)

Cascode amps

gain, bandwidth & stability, I/O range/swing.

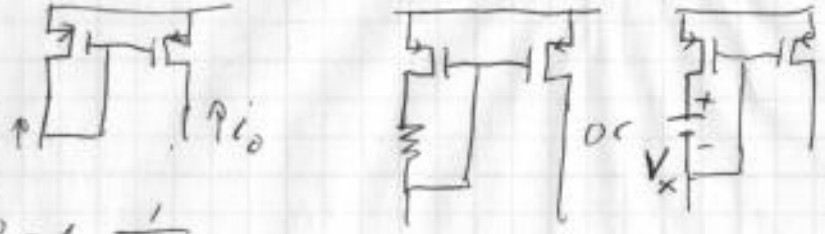
Simplest

telescopic cascode

(slide scanned in last lecture)

W10L1

High-swing cascode mirros



$\frac{i_o}{i_i} = 1 \frac{1}{1 + s/\omega_{pn}}$

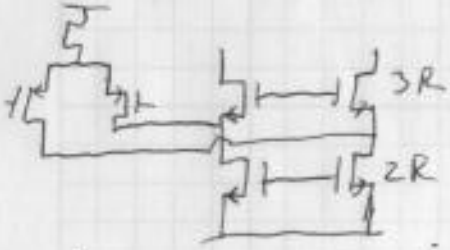
how big can R be and still have FET in saturation?

how big can V_x be? V_{tp}

$I_D R < V_{tp}$ is fine

W10L1 | 4/5/04

Lets look at NMOS biasing



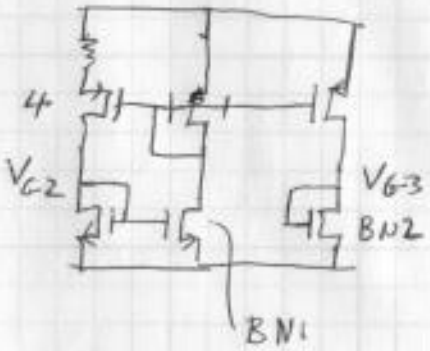
to maximize swing

choose V_{ov2} as small as possible (100mV for this class)

$\Rightarrow V_{G2} = V_{tn} + V_{ov2}$

Choose V_{G3} s.t. $V_{S3} = V_{D2} \approx V_{ov2}$

$V_{G3} = V_{tn} + V_{ov3} + V_{ov2} + \text{margin}$



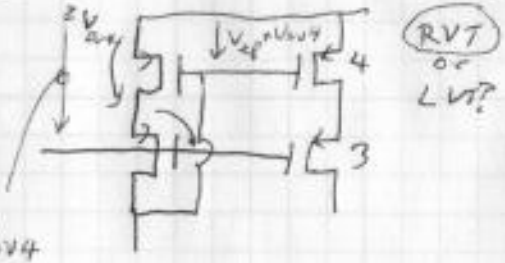
if $\left(\frac{W}{L}\right)_{BN2} = \frac{1}{4}\left(\frac{W}{L}\right)_{BN1}$

then $V_{ov_{BN2}} \overset{?}{=} V_{ov_{BN1}}$

if currents are same, then 2

Safer to choose $\frac{1}{5}, \frac{1}{6}$

use some trick for PMOS mirror



$V_{tp} + 2V_{ov4}$

why does this still work as a mirror?

what is the gain from V_{G4} to V_{S3}?

$G_m \approx g_{m4}$ $R_O \approx \frac{1}{g_{m3}}$

$A_v = -\frac{g_{m4}}{g_{m3}} = -1$

4LR specify the current

3LR let it flow through

why do we need 3L?

Don't, but keeps V_{D4LR} same

" I_{D4LR} same