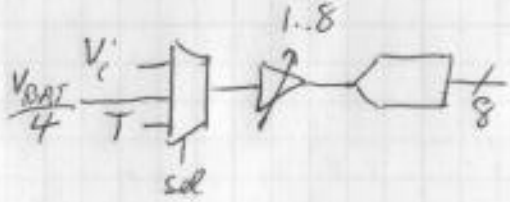
Project
teams of 3 - prefer 140/240 segregation
meetings next week



Switched Caps
capacitor basics
settling
PGA
ADC
switches

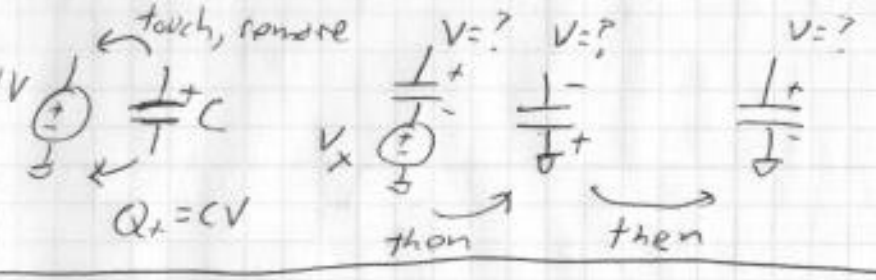
Capacitors $Q = CV$

actually $Q_+ = CV$

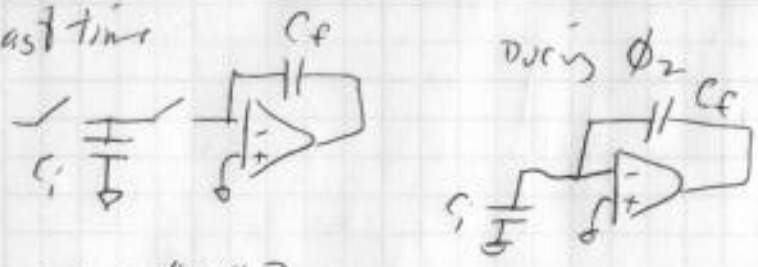
$Q_- = -Q_+$

Real caps have parasitics - cap to ground
- series R
- parallel R

we ignore (240B)



Last time



what is "f"?

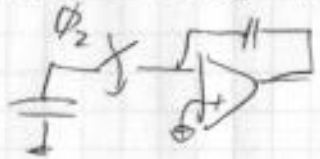
$$\frac{C_f}{C_i + C_f}$$

what is A_{CL}? (from where to where?)

$$\frac{C_i + C_f}{C_f} = 1 + \frac{C_i}{C_f}$$

not $\frac{C_i}{C_f}$ or $-\frac{C_i}{C_f}$ (which is the SC gain)

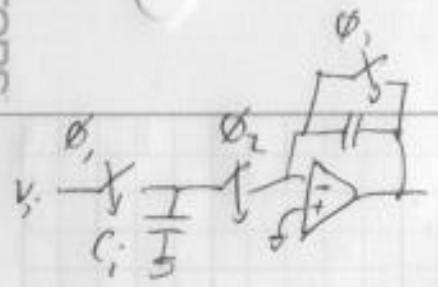
what is the time response?



how many τ for 0.1% settling?

(7 τ)

$\tau = \frac{1}{\omega_{pcl}}$ $\omega_{pcl} = f\omega_u$



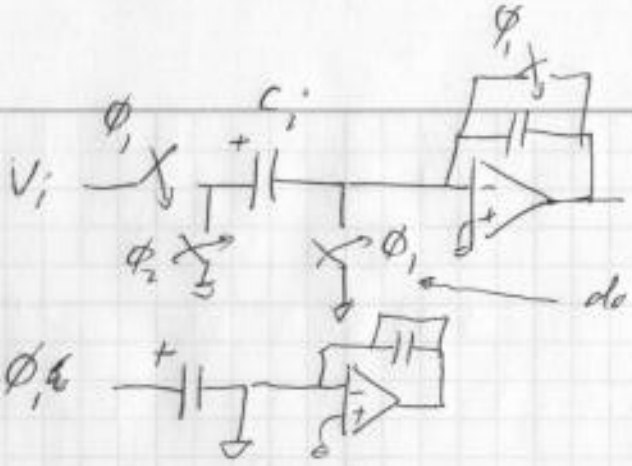
negative gain
need negative supply

what if I could flip C_i upside down?

$Q_{f,\phi_2} = -Q_{i-,\phi_1}$

$= C_i V_i$

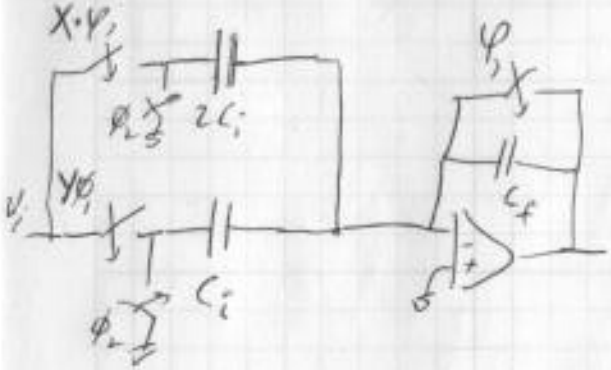
$Q_+ = C_i V_i$ $\quad Q_{i-,\phi_1} = -C_i V_i$ $\quad V_o = +\frac{C_i}{C_f} V_i$



do we need this cap?
no

$Q_{i+,\phi_1} = C_i V_i$ $\quad Q_{f+,\phi_1} = 0$

$Q_{i-,\phi_2} = 0$ $\quad Q_{f-,\phi_2} = -C_i V_i$



Programmable Gain Amps

$X=0,\ Y=1$ $\quad A = \frac{C_i}{C_f}$

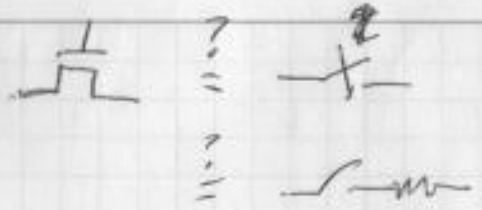
$X=1\ \ Y=0$ $\quad A = \frac{2C_i}{C_f}$

$X=1\ \ Y=1$ $\quad A = \frac{3C_i}{C_f}$

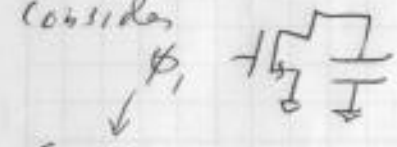
Amp specs

- ω_a st. get 7 τ settling in ADC input
- load cap is ADC input
- input common mode includes ground
  i.e. ground ±
- output swing to 0 - huh?!?
  during φ_1, and during φ_2

Switches

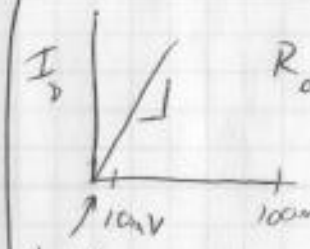


consider ϕ_1



$[0, V_{DD}]$

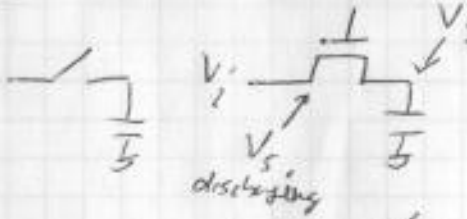
$\frac{dV_c}{dt} = \frac{I_D}{C} = \frac{1}{C}$ { $\mu_n C_{ox}$ W/L V_{GS} V_t V_{DS} ; $\frac{\mu_n C_{ox}}{2}$ }



$R_{ON} = \frac{V_{DS}}{I_{DS}} = \frac{V_{DS}}{\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_t - \frac{1}{2}V_{DS}\right)V_{DS}}$

$\approx \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{DD} - V_t\right)}$

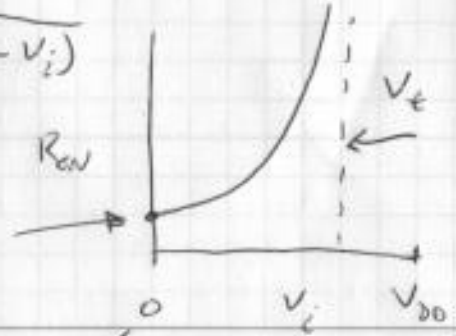
Spend most of the settling time in the lower left corner. So that is the slope that matters need to settle to $\frac{1}{2}$ LSB



$V_{GS} = V_{DD} - V_i$

now $I_D = \mu_n C_{ox} \frac{W}{L}\left(V_{DD} - V_i - V_t - \frac{1}{2}V_{DS}\right)V_{DS}$

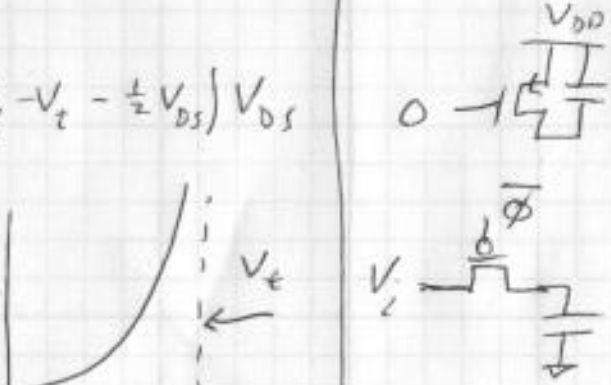
$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{DD} - V_t - V_i\right)}$



Body effect makes this worse (V_t bigger w/ $V_{SB} > 0$)

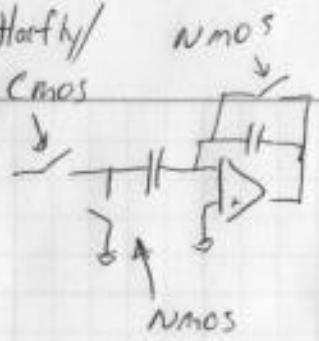
NMOS devices will not pull above $= V_{DD} - V_{tn}$

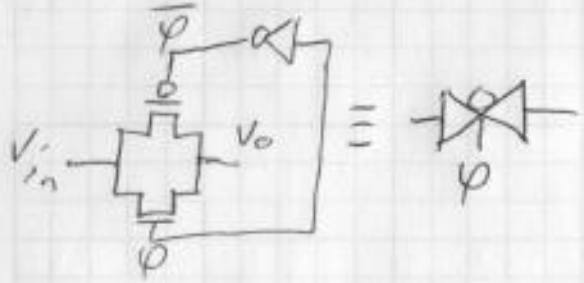
PMOS devices will



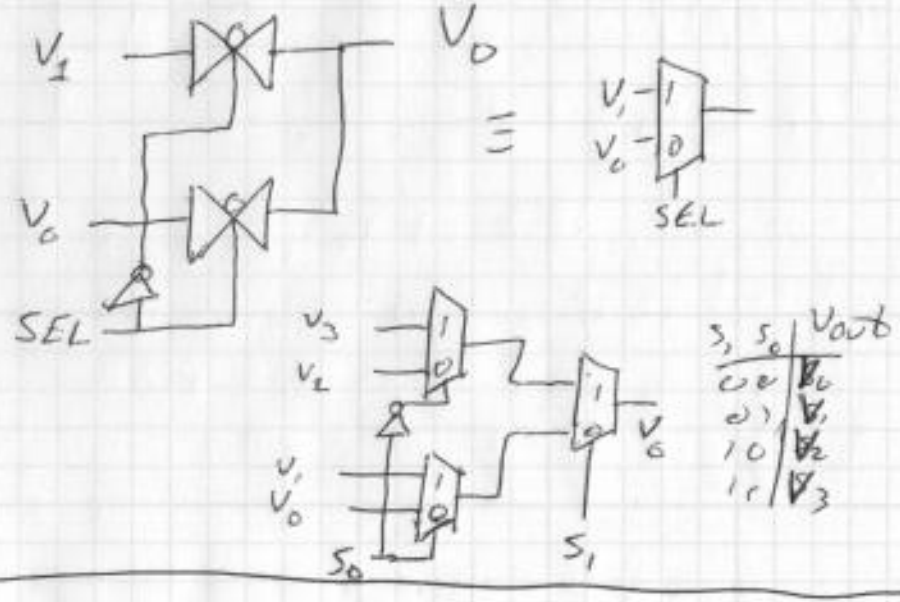
SPOTS

Pulling low NMOS
pulling high PMOS
could be either: butterfly

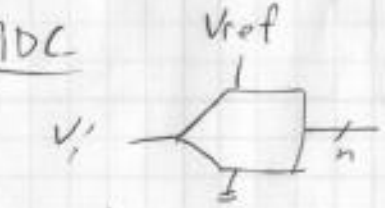


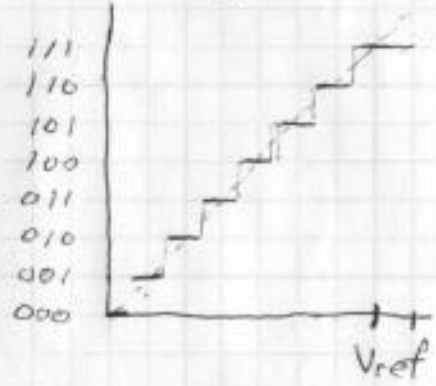


Analog MUX



ADC



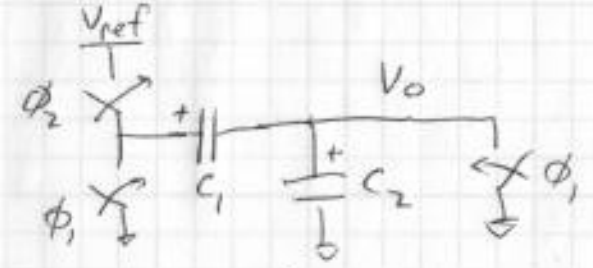


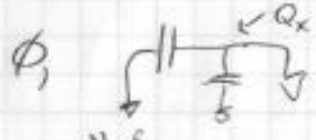
$$1LSB = \frac{V_{ref}}{2^n} = \frac{1V}{2^8} \approx 4mV$$

ideally a digital value "3" corresponds to

$$V_{in} = V_{ref}\frac{b}{2^n} \pm \frac{V_{ref}}{2^{n+1}}$$

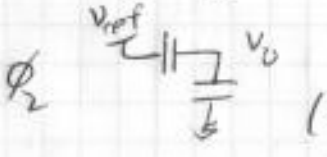
Building Block: CAP DAC





$Q_x = Q_{1-} + Q_{2-}$

$Q_{1-} = Q_{2-} = 0$ $\quad Q_x = 0$



$$Q_x = -C_1(V_{ref} - V_x) + V_{ref}C_2 = 0$$

$$(C_1 + C_2)V_x = C_1 V_{ref}$$

$$V_x = \frac{C_1}{C_1 + C_2} V_{ref}.$$