Project terms of 3 - prepare 140/240 segregation matrices last week

Switched Caps
- capacitor basics
- settling
- PGA
- ADC
- switches

Capacitors
- $Q = CV$
- $\frac{1}{T}$

Actually $Q_+ = CV$

Real caps have parasitics - cap to ground
We ignore (2408)

Series R
- parallel R

Realistic case:
- $V_0$
- $\frac{1}{C}$
- $V_+$
- $V_-$
- $Q_+ = CV$

Then
- $V_+$
- $V_-$

Last time
- $C_f$
- During $\Phi_2$
- $C_f$

What is $f$?
- $\frac{C_f}{C_i + C_f}$

What is $R_{eq}$?
- (from where to where?)
- $\frac{C_i + C_f}{C_f} = 1 + \frac{C_i}{C_f}$

Note:
- $\frac{C_i}{C_f}$ or $-\frac{C_i}{C_f}$ (which is the SC gain)

What is the time response?
- $\Phi_2$
- $\frac{V}{V}$
- $e^{-t/\tau}$
- How many $\tau$ for 0.1% settle?

$\tau = V_{pcc}$

$V_{pcc} = 0.1V$
negative gain
need negative supply
what if I could flip $C_i$ upside down?

$V_i = \frac{1}{2}$

$q_0 = \frac{1}{2} V_i$

$q_1 = C_i V_i$

$q_2 = -C_i V_i$

$q_3 = V_0 = \frac{1}{2} C_i V_i$

$\phi_1 = \frac{1}{2}$

$q_4 = -q_0$

$q_5 = -q_1$

$q_6 = -q_2$

$q_7 = -q_3$

amp specs
- when std. set $V_2$ settling in ADC input
- load cap is ADC input
- input common node includes ground
- output swing to 0 - huck!!!
  - do $q_1$, nd do $q_2$
  - $A = \frac{C_i}{C_f}$
  - $A = \frac{2C_i}{C_f}$
  - $A = \frac{3C_i}{C_f}$
  - $A = \frac{C_i}{C_f}$

programmable gain amp

do we need this? no
Pulling low NMOS
Pulling high PMOS
Could be either: butterfly

Analog MUX

ADC

Build block: CAP DAC

Vref

1 LSB = \frac{V_{ref}}{2^n} = \frac{1V}{2^8} ≈ 4mV

Ideally a digital value

V_{in} = V_{ref} \frac{b}{2^n} + \frac{V_{ref}}{2^{n+1}}

V_X = \frac{C_2}{C_1 + C_2} V_{ref}