Project

groups

design
debugging

Analog MUX

Regulators

CAP DAC, ADC

Project groups: 2 or 3 people
140 240 separate

sign-up google doc (piazza)

Presentation: who you are
schematic
division of labor
schedule

Project design, debugging

- integrate as early as possible!
  use ideal components
  interfaces are the devil's playground!
- use hierarchy
  bias networks, cap arrays, switches
  debug separately
- use source code control (git?)

debug in small pieces

Discussing status

"X works" - meets all specs over all PVT corners. Design is completely done,

"is alive" - simulates with some resemblance to desired behavior

"broken" - Fundamental flaw

"has X perf at 25C over 1.8 to 3.6"

annotate and don't touch things that get to this level

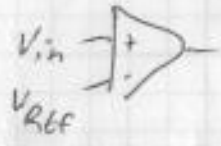
140/240A 19FA WIZL1

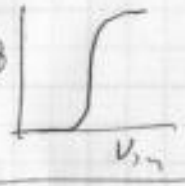
Debugging

Bias point voltages, currents, g_m, r_o } compare to hand calcs

DC sweeps } don't hack!

be careful of how you simulate high-gain amplifiers,



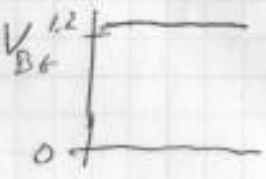


if $A_v = 10^4$ what is useful range of V_{in}?

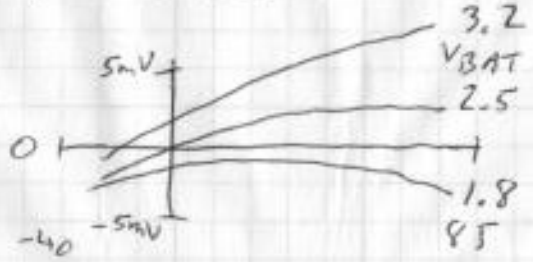
presenting results

- annotated schematics
- processed simulation results

"BC works" - only if everything works PVT

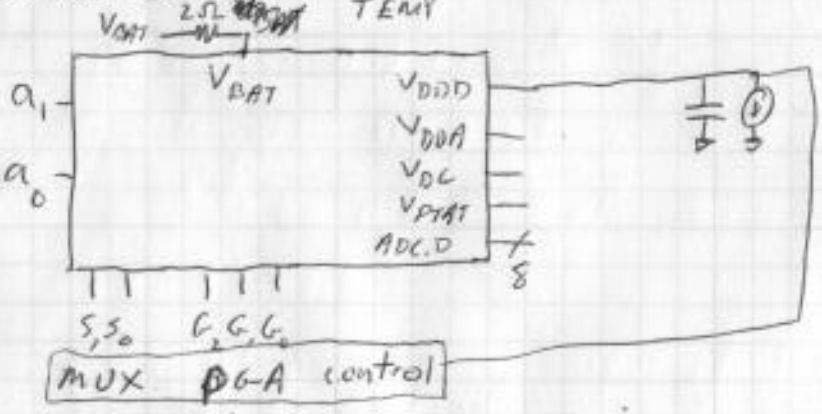


Better, but how good?



very helpful!

test harness

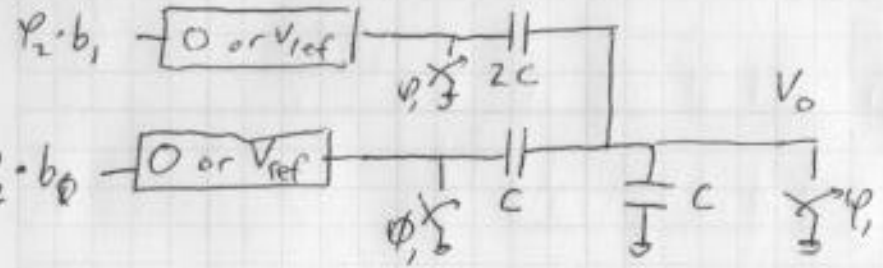


this is our interface to your design.

We will give you a SAR digital block

(See note WILLZP4

turn divider into a Voltage DAC



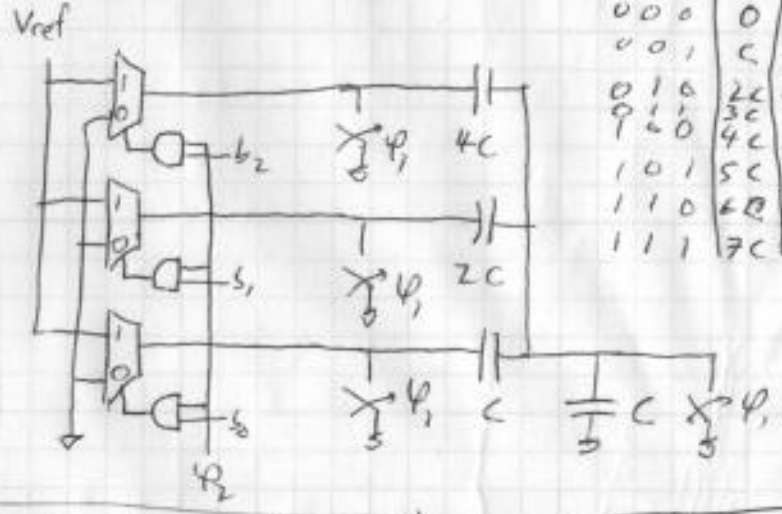
during φ_2:

$C_1 = B \cdot C$ B integer $\in [0, 2^n - 1]$

$C_2 = C + (2^n - 1 - B)C$

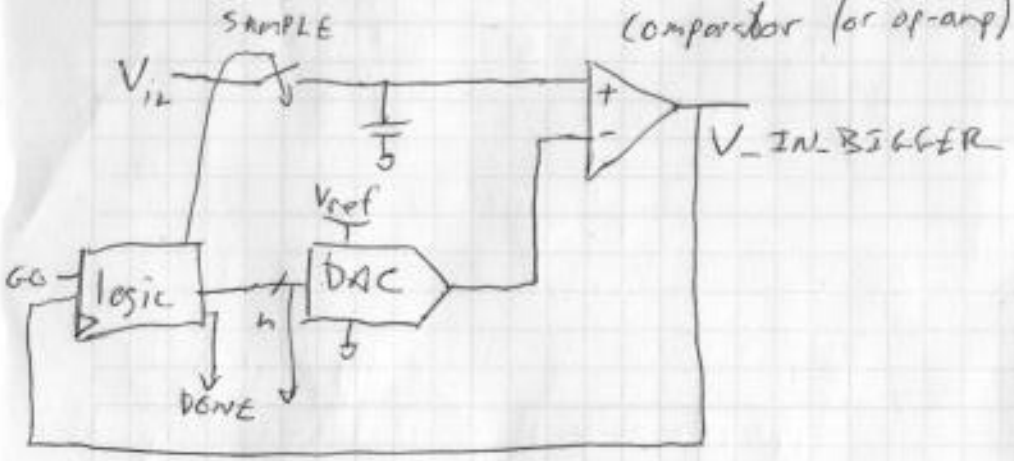
φ_2: $V_o = \frac{V_{ref} C_1}{C_1 + C_2} = \frac{BC}{BC + (2^n - 1 - B)C + C} = \frac{B}{2^n} V_{ref}$

Now we have a Voltage DAC implemented w/ a CAP DAC



$b_2 b_1 b_0$	C_1	C_2	V_{out}
0 0 0	0	8C	0 V_{ref}
0 0 1	C	7C	$\frac{1}{8} V_{ref}$
0 1 0	2C	6C	
0 1 1	3C	5C	
1 0 0	4C	4C	$\frac{1}{2} V_{ref}$
1 0 1	5C	3C	
1 1 0	6C	2C	
1 1 1	7C	C	$\frac{7}{8} V_{ref}$

How to make an ADC?



simplest logic: counter.

count until V_IN_BIGGER goes low.

counter is slow (and variable)

binary search is fast

```
set b_i = 0  ∀ i ∈ [0, n-1]
for i = n-1, i ≥ 0, i-- {
    set b_i = 1
    wait
    if (V_IN_BIGGER == 0) set b_i = 0
}
```

sample input

make n compares

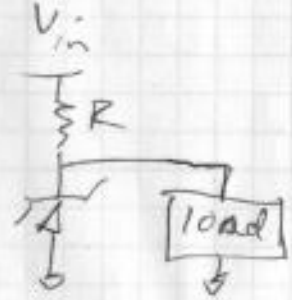
result is ready

Problem: building the comparator.

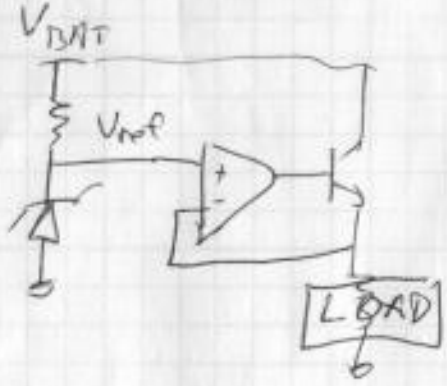
Double, but input offset varies over CM input range.

prefer to compare all 1 voltage.

Regulator early

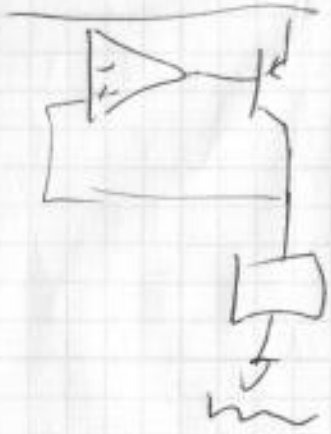


Wastes a lot of power



but need at least $V_{BE,on}$ (or $V_{th}+V_{ov}$)
+ more if op-amp has swing issues

Low drop-out



negative gain