Problem 2: compare \( O \) to \( V_{ref} \). What will be the output for \( V_i = 0 \) and \( V_i = \frac{B}{2} \)?

Do we need \( q_1 \) and \( q_2 \)? What if \( q_1 = 0 \) during \( q_2 \)?

\[ V_i = V_{ref} \]

\[ V_{out} = V_i - V_{ref} \]

ADC

Switches and bias circuits

Project: 3rd-FSM

Vin: stable - 1st integration

Sample

Pin: VIN

Vref:

Sample

Vin: 0V

Vin: PVA drive to 0

Sample

Vin: B

0V
Can we set \( V_{id} = V_{in} - \frac{B}{2} V_{ref} + \frac{1}{2} V_{ref} \)? Yes, w/ SC compliance.

Recall what if done for \( V_{id} \) across all of these caps?

Then doing \( V_{id} \) for \( V_{o} = \frac{B}{2} V_{ref} + V_{c} \)

How do we think?
Note that $V_1$ needs to be above $V_{REF}$

during $b_2$
test.

What if $V_{IN}$ were 0V?

$V_{OUT} = V_{REF} - 0.5V$

$V_{OUT} = V_{REF} + 0.5V$

if switches are in Volen power domain

this forward biases the DB diode in PMOS

Do not forget to switch $V_{OUT}$ if you
only use 2 stages.

Used to pull low. Device N MOS?

Refer to pull low. Device N MOS.

what is $V_{IN}$, 0V only?

If $V_{IN}$ leads to high, will it settle there?

PGA - pull $V_{OUT}$ to ground

need to pull to 0V? No, $<< 4 V$

$V_{OUT}$ will not sit in saturate. Build

$V_{OUT}$ probably need 2-4 stages.

$V_{OUT}$ probably need 2-4 stages.

PGA stage F at 0V will be used.

N MOS?
If load power off, V1(V0) = 0V.

If load power on, FC operating?

Turn off power: 100mV < 200mV.

AV = 100mV

A = (100mV)/(200mV)

More switch issues

PEA Q2

ADC 0x-1

Charge injection