Project - signups MTu

Presn: Schedule - 1st interaction

ADC

binary search

compare to V_{DD}

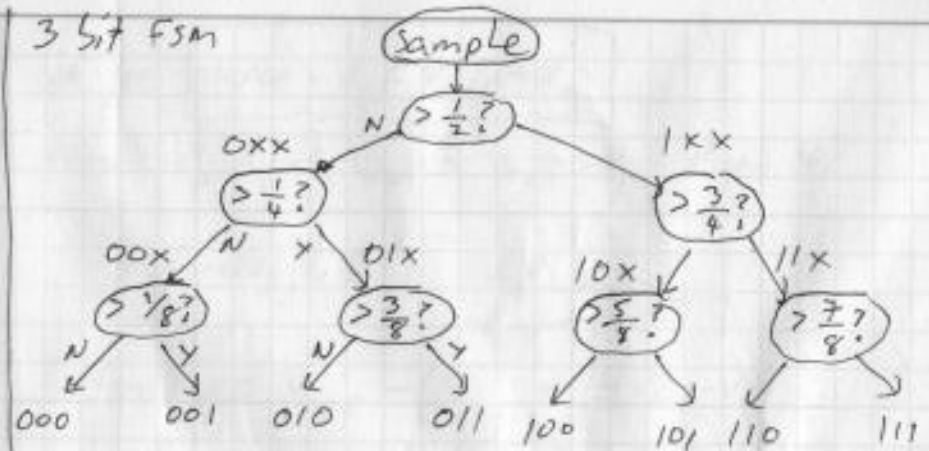
PGA

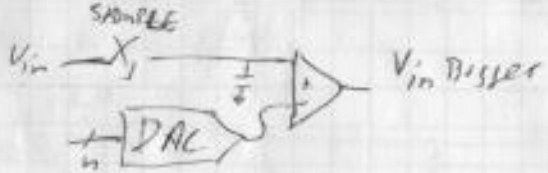
drive to 0

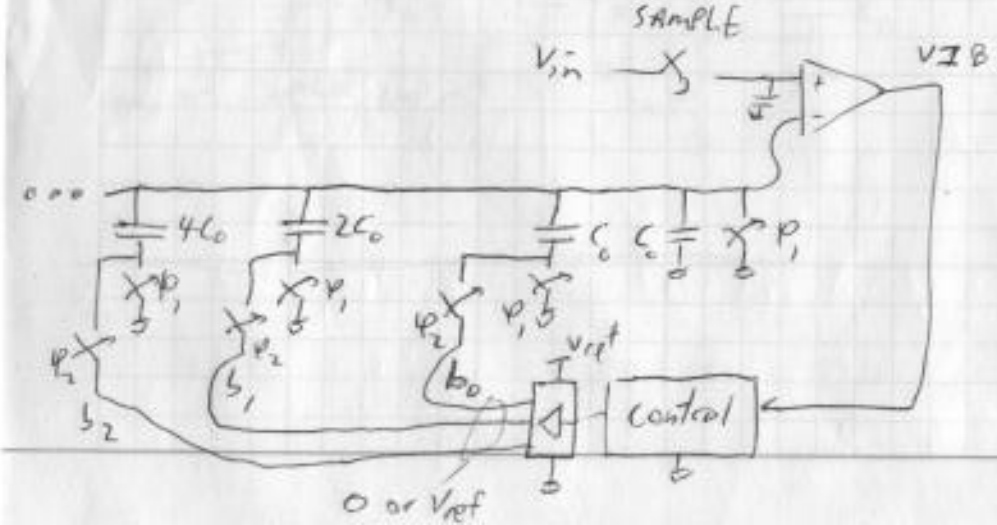
switches

fwd biasing diodes

3 bit FSM







Problem: compare 0 to V_{ref}

maybe a PMOS input FC.

what supply voltage to set V_{icm} [0, V_{ref}]

Do we need ϕ_1 and ϕ_2?

what if fsm writes B=0 during ϕ_1?

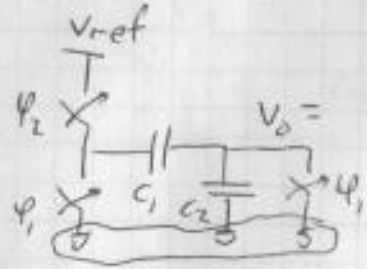
what if replace ϕ_1 with SAMPLE?

$V_- = \frac{B}{2^n} V_{ref}$

$V_{id} = V_+ - V_- = V_{in} - \frac{B}{2^n} V_{ref}$

Can we set $V_{id} = V_{in} - \frac{B}{2^n} V_{ref}$ at the same CM input? Yes, w/ SC cleverness.

Recall



$V_o = \frac{C_1}{C_1+C_2} V_{ref} = \frac{B}{2^n} V_{ref}$

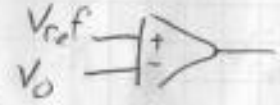
what if during φ_1 ~~we put~~ we put V_z across all of those caps

then during φ_2 we'd set $V_o = \frac{B}{2^n} V_{ref} + V_z$

if we choose $V_z = V_{ref} - V_{in}$

then $V_o = \frac{B}{2^n} V_{ref} + V_{ref} - V_{in}$ during φ_2

and finally, if

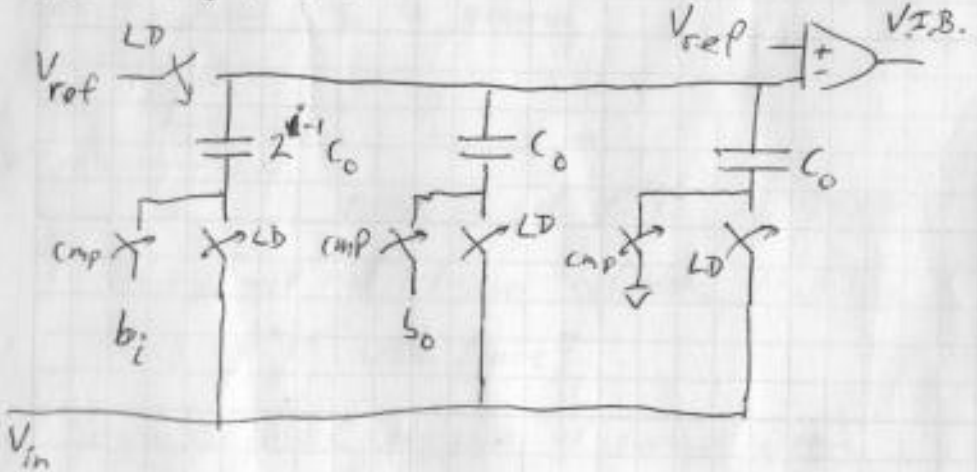


then $V_{id} = V_{ref} - \left(V_{ref} + \frac{B}{2^n} V_{ref} - V_{in}\right)$

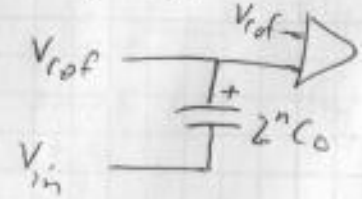
$= V_{in} - \frac{B}{2^n} V_{ref}$

just like before! (w/ZLZ p/LR)

How to do that?

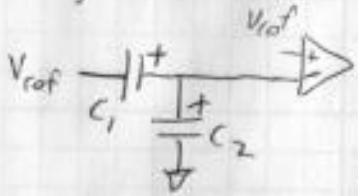


During LD



$Q_{LD} = (V_{ref} - V_{in}) 2^n C_0$

During CMP



$C_1 = BC_0$

$C_2 = (2^n - B)C_0$

$Q_{cmp} = (V_o - V_{ref}) C_1 + V_o C_2$

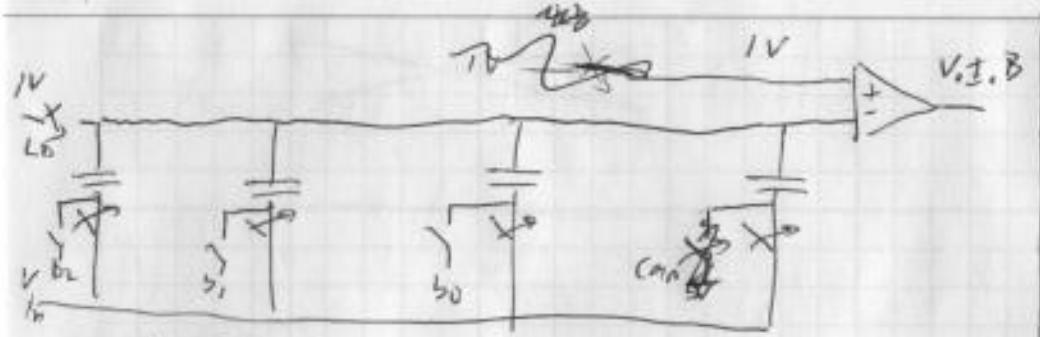
$= (C_1 + C_2) V_o - C_1 V_{ref}$

must $= Q_{LD} = (V_{ref} - V_{in}) 2^n C_0$

$2^n C_0 V_o - BC_0 V_{ref} = 2^n C_0 (V_{ref} - V_{in})$

$V_o = \frac{B}{2^n} V_{ref} + V_{ref} - V_{in}$

$V_{id} = V_+ - V_- = V_{in} - \frac{B}{2^n} V_{ref}$



Note that V_- went above V_{ref} during b_2 test.

What if V_{in} were 0?

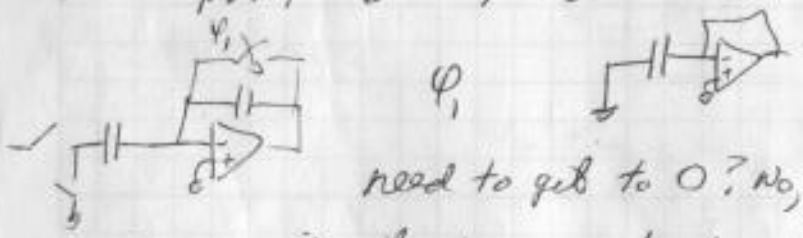
during LD, caps set $V_- = V_{ref} - 0$

during cmp, b_2: $V_- = V_{ref} + \frac{1}{2} V_{ref}$

$= 1.5\ V$

if switches are in V_{DDA} power domain this forward-biases the DB diode in PMOS

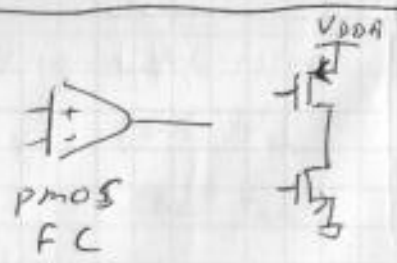
PGA - pulling V_o to ground



need to get to 0? No, << 4mV

op-amp will not stay in saturation that low, but will it settle there?

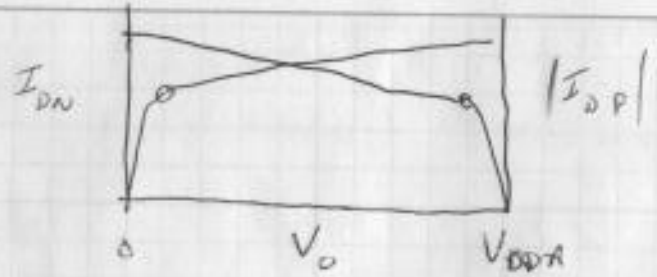
Single stage FC maybe w/ careful design but probably need 2nd stage

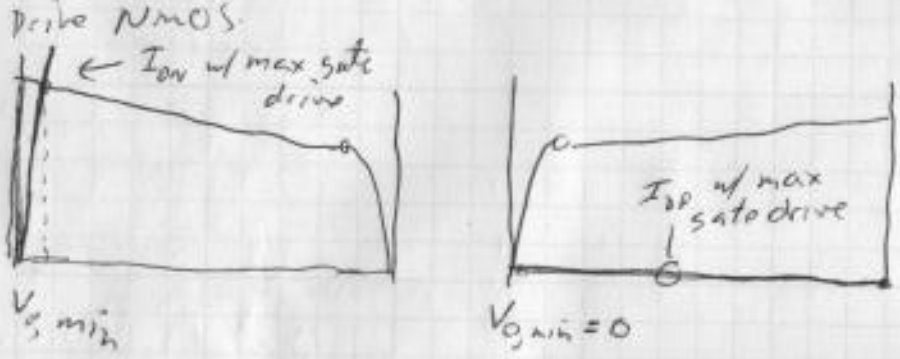


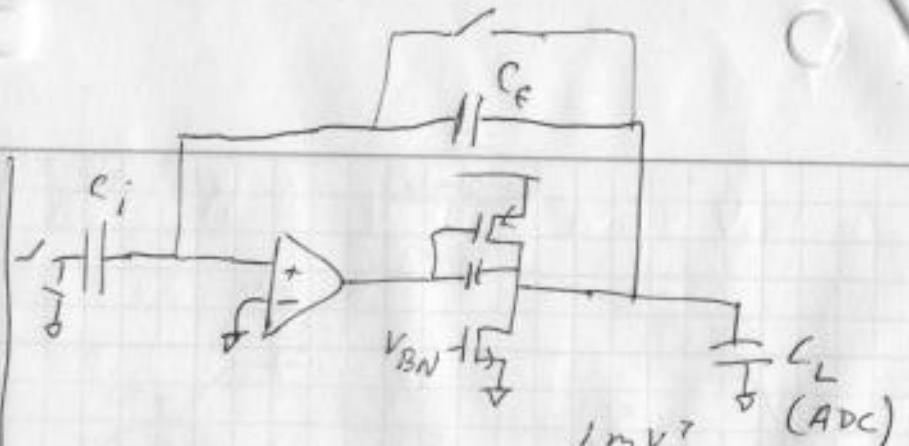
Don't forget to switch V_+, V_- if you add a 2nd stage.

Want to pull low. Drive NMOS? PMOS? both?

Will need to compensate (now a 2 stage)







1mV?

if want PMOS off w/ 0.1mV on V_o

What gain needed in FC op-amp?

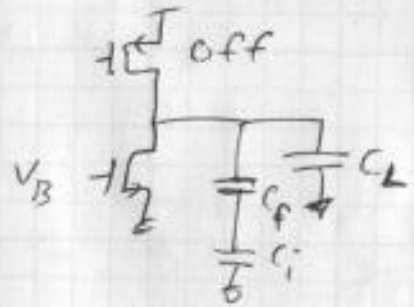
turn off PMOS: 100mV? 200mV?

$AV_{id,FC} \geq 100mV$

$A \geq \frac{100mV}{0.1 \text{ to } 1mV} \rightarrow (100 \rightarrow 1000)$ A_{FC}

Switch

Settling time



More switch issues

PGA ϕ_2

ADC b_{n-1}

charge injection