Project

2nd presentation Dec 2, 3 Dec 4, 6 Appl lecture, me

No, 20, 22 WF me Thanksgiving

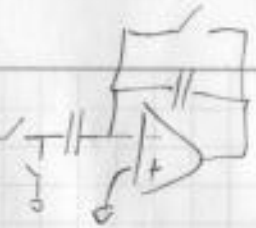
Final presen RRR week

Driving output to ground

Charge injection

Strong ARM

PGA

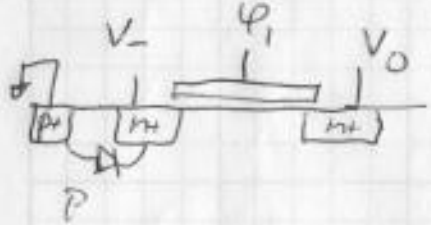


φ_1: drive output to ground : << 1LSB

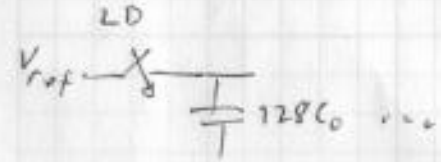
φ_2: amplify accurately [0, 1], error << LSB

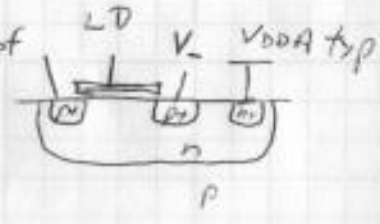
see note W12 L2, p 3 & 4

FWD bias switches

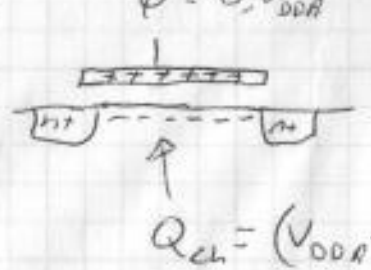


ADC





Charge injection



$Q_{ch} = (V_{DDA} - V_{th}) C_{ox} WL$

fast falling edge: assume $\frac{1}{2} Q_{ch}$ goes each side

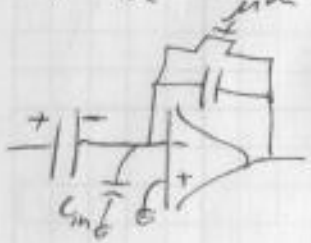
slow falling edge: channel charge goes to source

but

$Q_{od} = V_{th} C'_{ox} W$

channel sore at V_{th}

say $C_{ol}' = 1\frac{fF}{\mu m}$ $W = 1\mu m$ $C_{ol} = 1fF$



φ_1: $Q_- = -V_{in} C_1 + V_- C_{in} + (V_- - V_o) C_2 \} \approx 0$

$+ -V_{DDA} C_{ol}$

Slowly drop φ_1 and this term reduces to $-V_{th} C_{ol}$

φ_2: $V_o = \frac{-Q_-}{C_2} = \frac{C_1}{C_2} V_{in} + \frac{C_{ol}}{C_2} V_{th}$

choose minimum $C_2 = 4fF$, neg V_{th} device

$V_o = \frac{C_1}{C_2} V_{in} + \underbrace{\frac{1fF}{4fF}(0.6V)}$

150mV error!

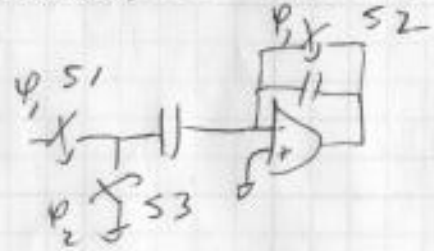
many clever ways to improve

simplest is to make $C_2 \gg C_{ol}$

if $C_2 = 100fF$, error = 6mV

make switch small, C_2 big $\Rightarrow$ slow response

what about other switches?



if S1 turns off before S2 $\Rightarrow$ problem

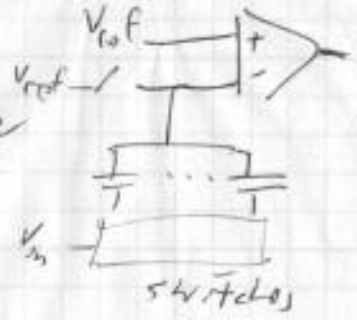
Q_{1+} gets extra charge

delay S1 rel S2: φ_1 $\overline{\varphi_1}$ S_2 S_1

φ_2 injection affects ADC

ADC comparator

Fine to use op-amp



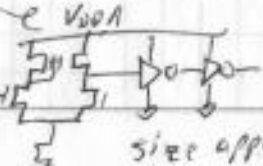
compare w/ V_{ref}

$\Rightarrow$ NMOS input

like $V_{id} << LSB$ to create clear 0, 1 output

$A_V \sim 1000$ or more

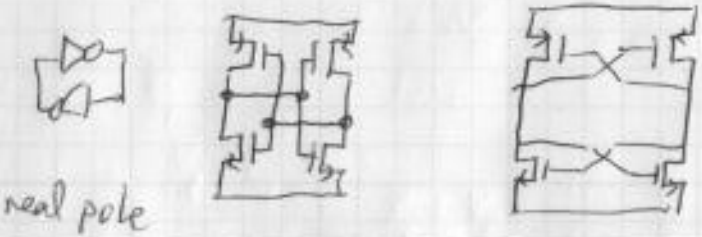
want digital output



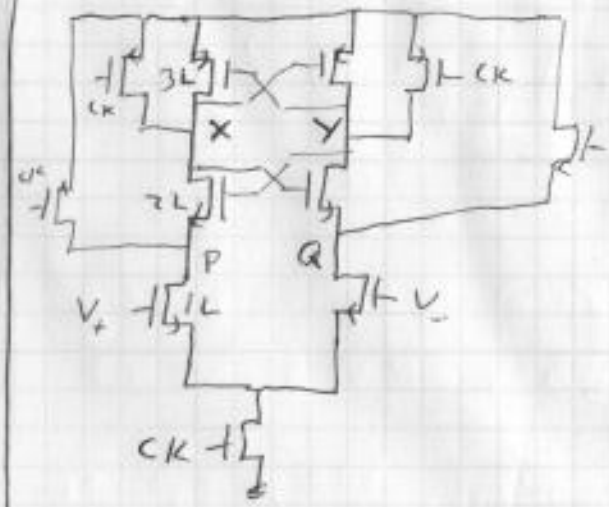
Strong ARM latch

- clocked comparator
- faster, lower power than op-amp-based
- easy to trim input offset.

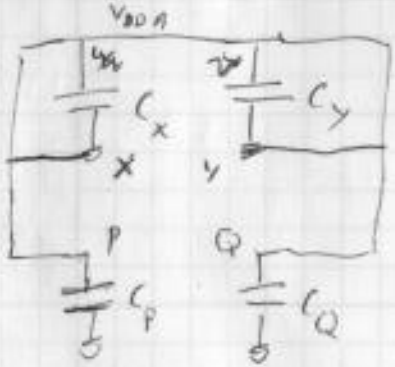
core element: cross-coupled inverters



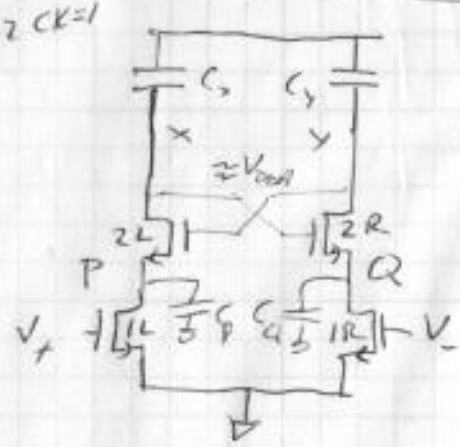
RHP real pole



Phase 1, CK=0



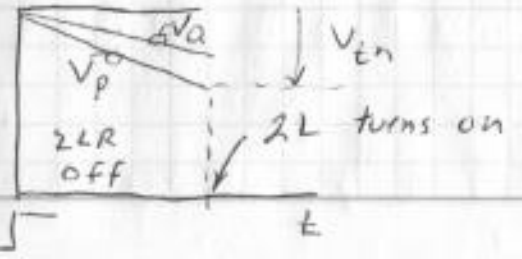
Phase CK=1

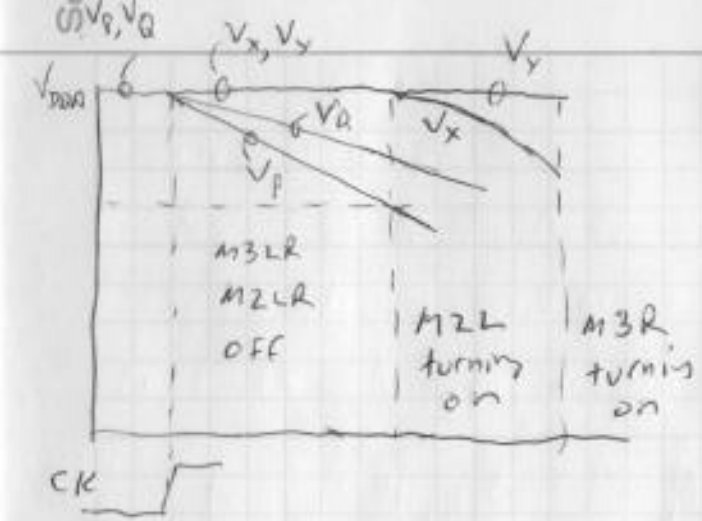


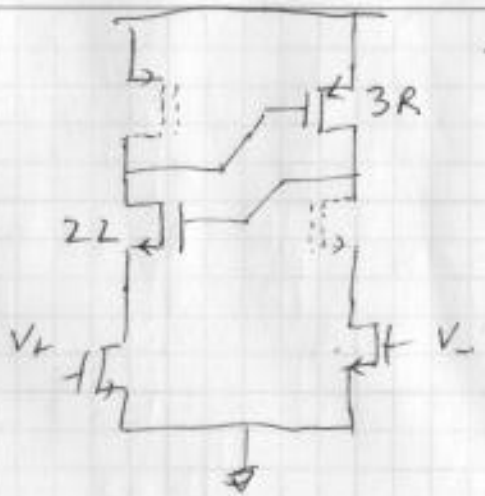
say $V_+ > V_-$

$I_{DL} > I_{DR}$

Phase CK=1

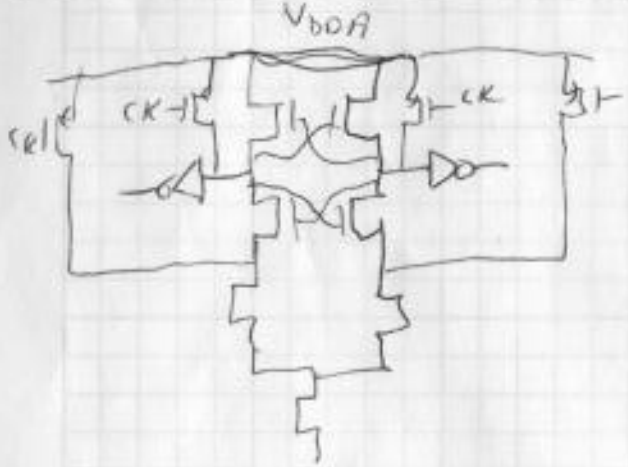






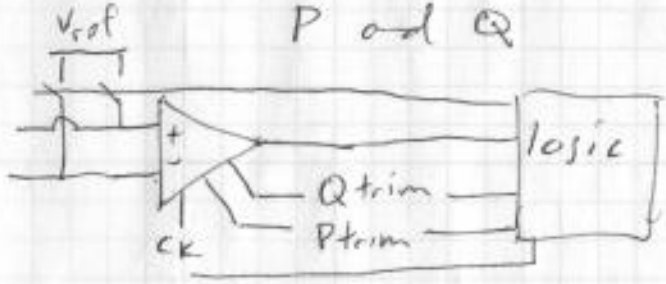
3R ON Keeps
3L OFF
2R ON

2L ON Keeps
3R ON
2R OFF



Add output buffers to locally to keep
$C_p \approx C_Q$

StrongRAM
Switches fast - order safe delay
rail-to-rail outputs
run auto-trim at boot!
- add small CAPDAC at both P and Q



compare 1000 times, if unbalanced result, trim CAPDACs