Flip-flops sample the input D on a rising edge of CK. A combination of logic ensures proper operation.

Result: based on leakage spikes on rising edges, Qspike is small. CV + crowbars

Project

Digital Circuits

Flip-flops circuit

Prominent interface

Circuit 1

Circuit 2

Circuit 3

Circuit 4

Circuit 5

Circuit 6
\[ Q = CV \quad A \quad V_{\text{spike}} = \frac{QR}{c} = \frac{0.16\text{mC}}{1\text{nF}} = 0.16\text{V} \]

\[ \approx 10\% \text{ supply} \]

2. Stage poles

2 extremes:

1) op-amp very slow,
   Pass gate tracks average current
   (as just discussed)

2) op-amp very fast
   Pass gate & control track demand.

\[ \frac{2.6\text{mA}}{10\text{mHz}} = \frac{260\text{mA}}{\text{mHz}} \quad \text{above right for } 0.18\text{Hz} \]

\[ (100\text{kHz}) (10 \frac{\text{mA}}{\text{s}}) = 1\text{F} \]

\[ \text{most don't switch on any siren} \]

\[ 2.6\text{mA const} \]

\[ \frac{160\text{mV}}{2.4\text{mA}} \]

\[ \frac{-2.4\text{mA}}{1\text{NF}} \]

IF DREC tracks desired demand perfectly

(Case 2) then \( V_{\text{DAR}} \) varies by

\[ (2.52)(4\text{mA}) = 8\text{mV} \]

trouble? Depends on "Power Supply Rejection" at low frequencies, feedback loop will counteract effect of supply on output. \( V_{\text{DAR}} \)

Above unity gain, will show up \( \pi \) directly.