Midterm - graded!

Midterm 2 -

Lecture W5L1 - taping now. HW5p1

Op-amps
- History
- structure
- CMOS 2 stage
  - current mirror

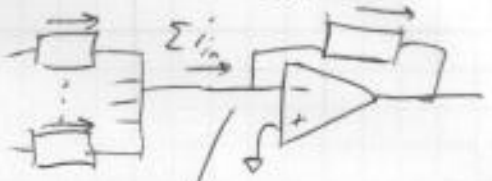
Mathematical operation amplifier

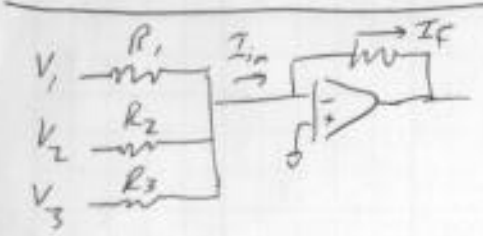
before widespread digital computers (~1980)

only way to do computation - Apollo

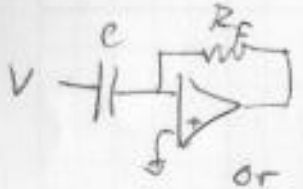
Today sometimes the best way.

Common building block: summing amp.



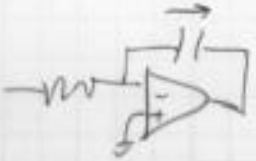


$$V_o = -I_f R_f$$
$$= -I_{in} R_f$$
$$= -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) R_f$$



$$V_o = I_f R = -I_1 R = -C\frac{dV}{dt} R_f$$

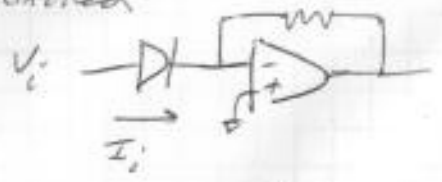
or $\frac{V_o}{V_i} = -sRC$



$$V_o = -\int_0^t I_f(\tau)/C \, d\tau + V_o(0)$$
$$= \frac{-1}{RC}\int_0^t V(\tau) d\tau + V_o(0)$$

or $\frac{V_o}{V_i} = \frac{1}{sRC}$ ODE!

Nonlinear



$$V_o = -I_i R_f$$
$$= -\left(I_s e^{V_{in}/V_{TH}}\right) R_f$$

$$V_o = -V_{TH} \ln \frac{I_i}{I_s}$$
$$= -V_{TH} \ln \frac{V_i/R}{I_s}$$

With a log table, even adders can multiply!

op-amp op-amp

$$A \cdot B = \exp\left(\ln(A \cdot B)\right) = \exp\left(\ln(A) + \ln(B)\right)$$

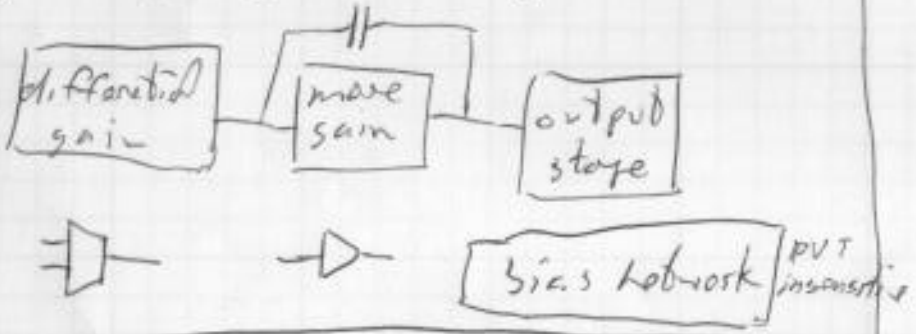
EGR 361 W5L1

How to make $\frac{1}{2}$?

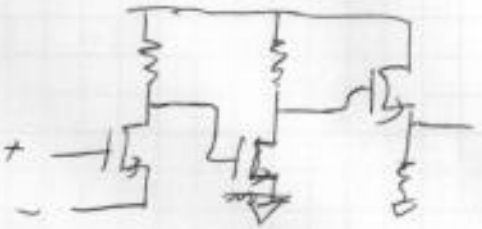
tubes - K2-W 1951

discrete NPN, NPN+PNP P65 1961
integrated NPN + ~~DNP~~ + PNP μA702 1963

Many/most shared similar design

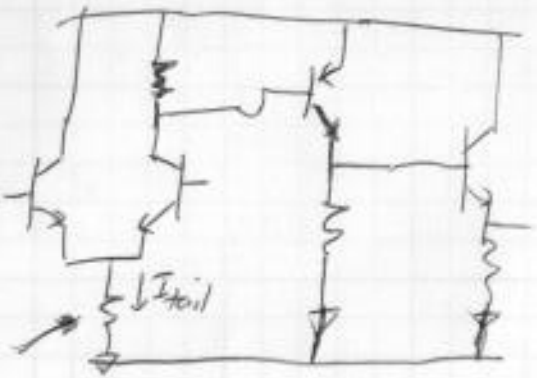


2 stage - lousy!



input offset, input resistance
gain variation, common mode rejection etc.

better

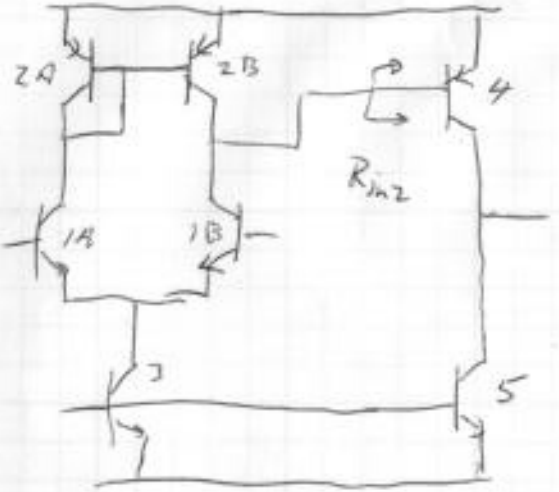


1936 patent

why NPN, PNP?

lots of variation w/ common mode input offset, power consumption gain, BW, output resistance

way better



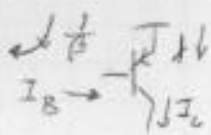
$$R_{in2} = r_{\pi 4} = \frac{\beta}{g_{m4}}$$
$$= \theta \frac{V_{TH}}{I_{C4}}$$
$$\approx \frac{2.5V}{I_{e4}}$$

compare to
$r_{o12} = \frac{V_A}{I_{C12}}$

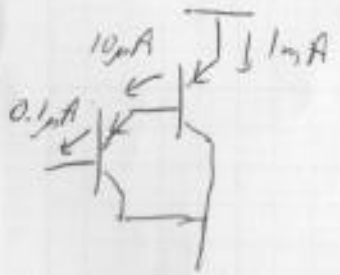
→ current mirror

→ Diode connected

How to increase $R_{in,2}$? Darlington



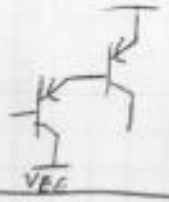
$I_c = \beta I_B$ $\quad \beta \approx 10 - 1{,}000$



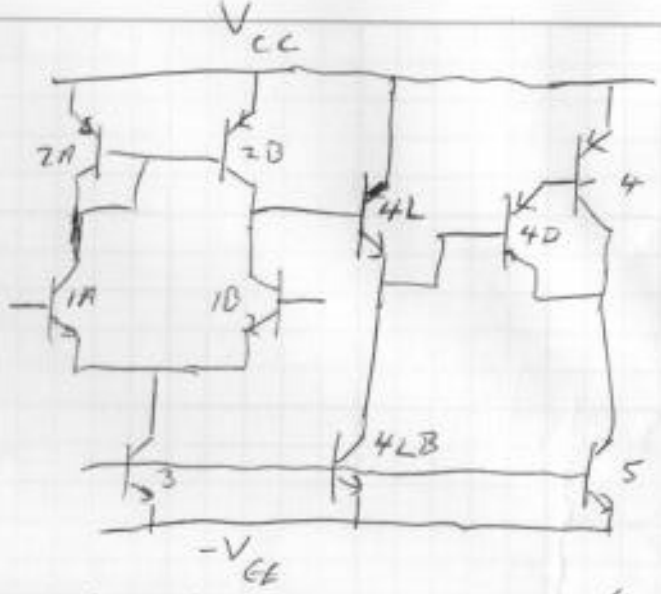
Darlington Pair

Affects bias point, output swing.

$V_{CE,sat} \rightarrow V_{BE} + V_{CE,sat}$

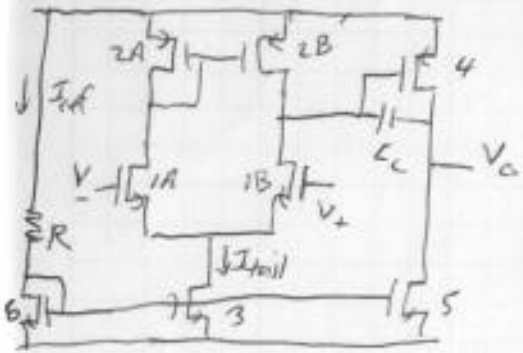


no swing effect.



Add Darlingtons on input pair (why?) and an output stage ⇒ LM324 (upside down)

CMOS Version - industry workhorse

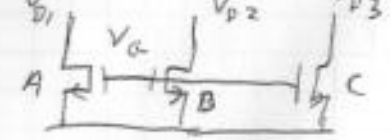


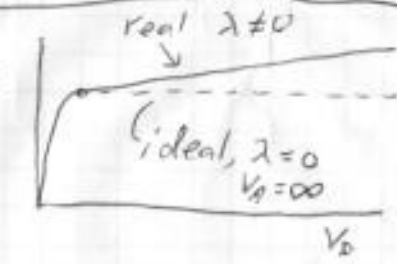
typically no output stage (good for driving capacitive loads - e.g. more CMOS)

1A,B	diff pair	$\frac{1}{2}I_{bias}$
2A,B	active load	
4	CS gain stage	I_{bias}
3,5,6	bias network	
R		

will replace soon

current mirrors





if A, B, C have same $\frac{W}{L}$, V_{GS}, V_t, $\mu_n C_{ox}$

they must live on the same I/V curve

Currents will be different if V_D are not the same

but only by $\frac{\Delta V_D}{V_A} = \lambda \Delta V_D$ o/o

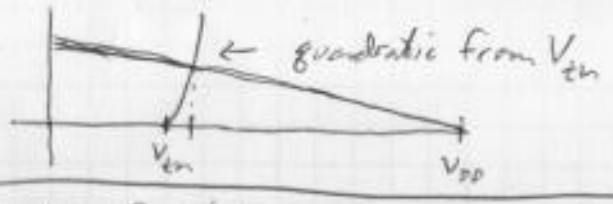
How to set V_G?

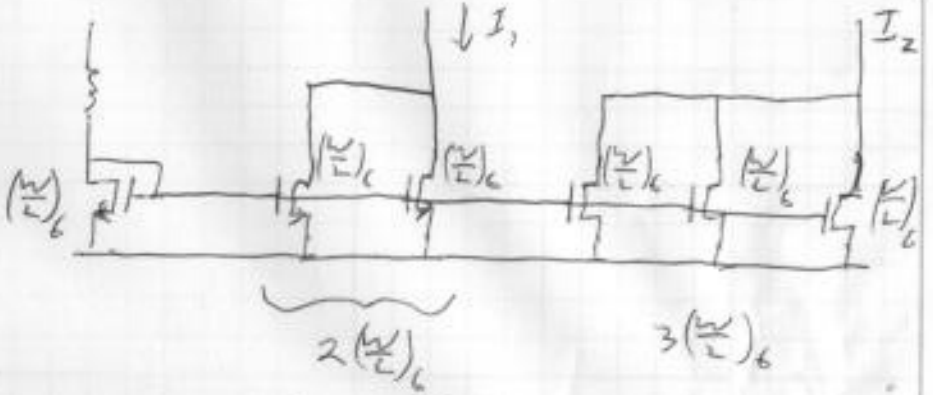
1) Generate reference current

2) shove through "Diode-connected" FET

$$I_{REF} = \frac{V_{DD} - [V_{th} + V_{ov}]}{R}$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{ov}^2 (1 + \lambda[V_{th} + V_{ov}])$$



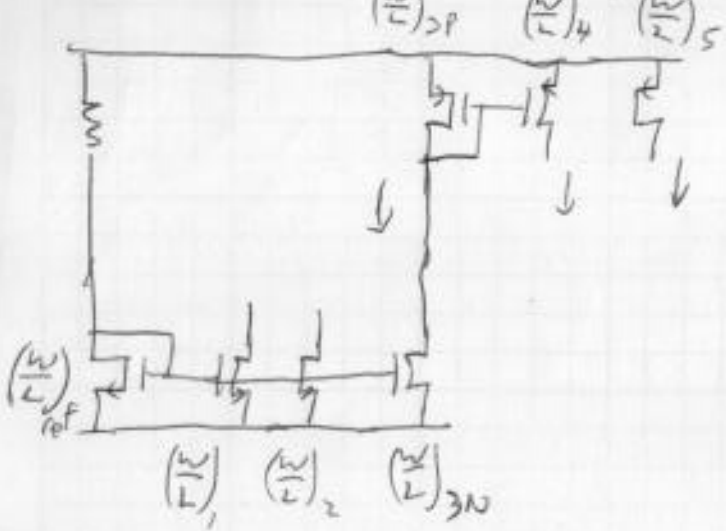


$$I_1 = 2 I_{ref} [1 + \lambda \Delta V_{D2}]$$

$$I_2 = 3 I_{ref} [1 + \lambda \Delta V_{D3}]$$

What is minimum voltage for V_{D2}, V_{D3}? V_{ov}

If you need sources & sinks, mirror away!



2 stage gain

1st stage: $G_{m1} = g_{m1} = \frac{2 I_{D1}}{V_{ov1}} = \frac{2(I_{tail}/2)}{V_{ov1}} = \frac{I_{tail}}{V_{ov1}}$

(not derived yet) → $R_{O1} = r_{o1b} \| r_{o2b} \approx \frac{r_{o12}}{2}$

$$A_{v1} = -G_{m1} R_{o1} = \frac{g_{m1} r_{o1}}{2}$$

2nd stage: $G_{m2} = g_{m4}$ $R_{O2} = r_{o4} \| r_{o5} \approx \frac{r_{o4}}{2}$

$$A_{v2} = -\frac{g_{m4} r_{o4}}{2}$$

$$A_{v0} = A_{v1} A_{v2} \approx \frac{1}{4} (g_{m1} r_{o1})(g_{m4} r_{o4})$$

[250, 100,000]