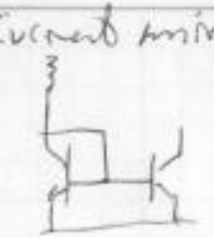
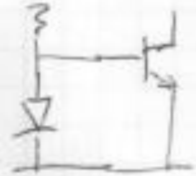
Regrindex
Mirrors,
Sources & sinks

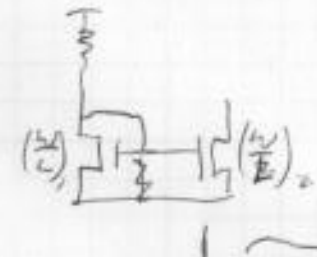
2 stage
sizing & bias
input range, output swing
differential gain
common mode gain

Current mirrors





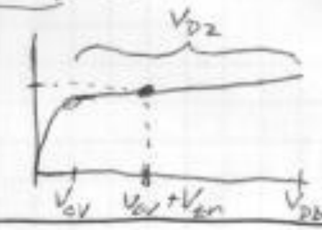
$I_{ref} = \frac{V_{CC} - 0.6}{R}$

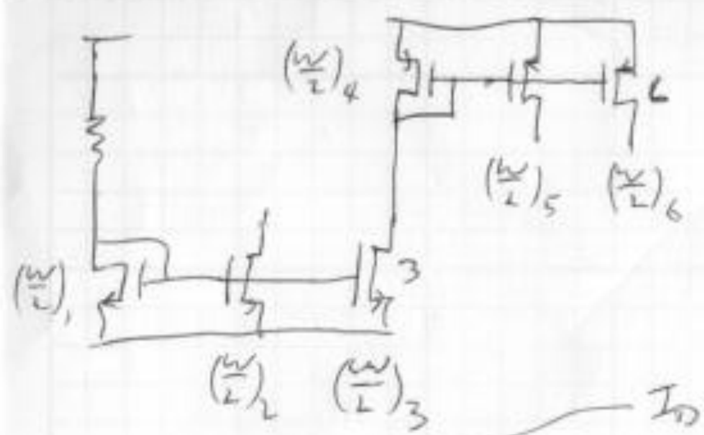


$I_1 \cong \frac{V_{DD} - (V_{tn} + V_{ov})}{R}$

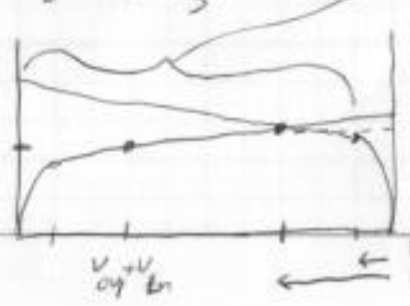
$I_2 = \frac{(W/L)_2}{(W/L)_1}\left(1 + \lambda \Delta V_D\right)$

may be negative

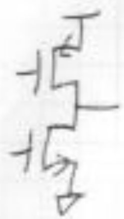




$I_{D5,6}$ live on this curve



<u>Feedback</u>



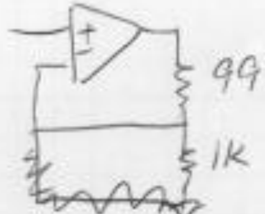
Say I want a gain of 100 $\pm 1\%$ from $V_{in} = 0$ to $10\,mV$
$V_{out} = 0$ to $1V$

can design for $A_v \cong 100$

~~[illegible]~~ are problem

<u>but</u>
1) input at 0? hard/impossible
2) r_o varies ore V_{out}
V_t, μC_{ox} varies w/ temperature
3) bias varies w/ supply
4) everything varies run-to-run and chip-to-chip (transistor to transistor)

compare to



ideal op-amp : $A_v = \frac{99k+1k}{1k}$

$= 100$

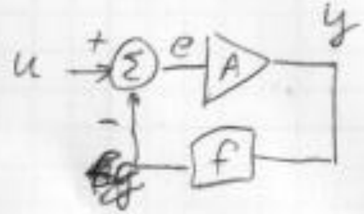
99 copies in layout

if careful, 0.1% matching

what if it's not an ideal op-amp?

input offset $\neq 0$
input current $\neq 0$
common mode gain $\neq 0$
differential gain $< \infty$

128 perspective



$y = Ae$

$= A(u - fy)$

$(1+Af)y = Au$

$H(s) = \frac{y}{u} = \frac{A}{1+Af} \approx 1/f$ if $Af \gg 1$

Finite A:

$H(s) = \frac{A}{1+Af} = \frac{A}{Af}\frac{1}{1+\frac{1}{Af}} = \frac{1}{f}\underbrace{\frac{1}{1+\frac{1}{(\text{loop gain})}}}_{\text{difference from 1 is error}}$

$\approx \frac{1}{f}\left(1 - \underbrace{\frac{1}{Af}}_{\%\ \text{error}}\right)$

need % error $< 1\% = 10^{-2} = \frac{1}{Af}$

$f = 10^{-2}$ also

need $A > \frac{1}{(\%\ \text{error spec})\, f} = \frac{1}{(10^{-2})(10^{-2})} = 10^4$

As long as $A > 10^4$ over

Process
Voltage (supply)
temperature
input/output swing

then Finite gain causes less than 1% error

Definitions

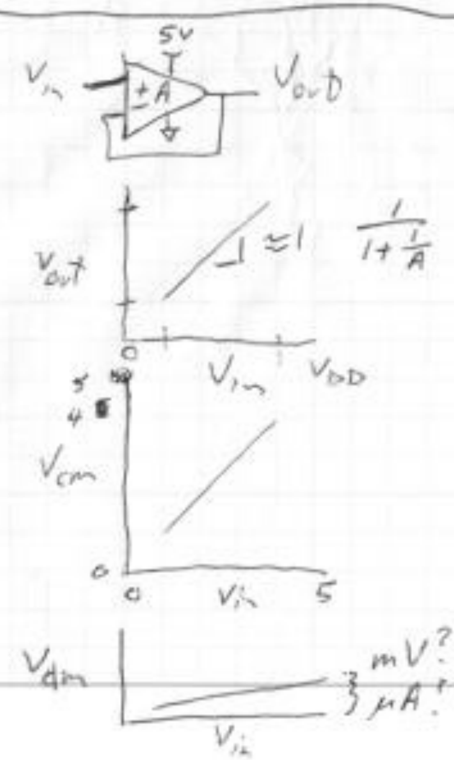
$V_{cm} = \frac{V_+ + V_-}{2}$

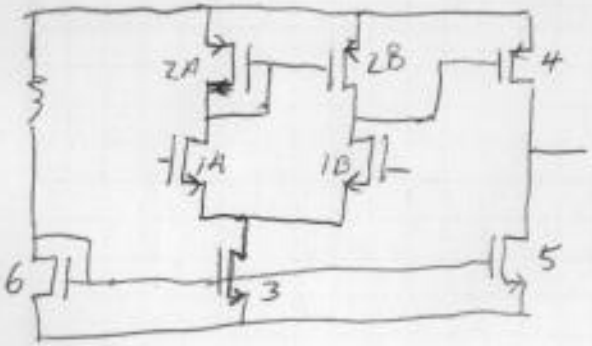
$V_{Dm} = V_+ - V_-$

A = op-amp gain

$T = Af$ = loop gain

$\frac{A}{1+Af}$ = closed loop gain





Device sizing/bias point

differential gain,
common mode gain
I/O range/swing

Sizing & bias

$I_{D2A} + I_{D2B} = I_{D3}$

the mirror sets up just the right gate voltage (V_{G2A}) to pass this current

This is also the DC bias point of V_{G4}

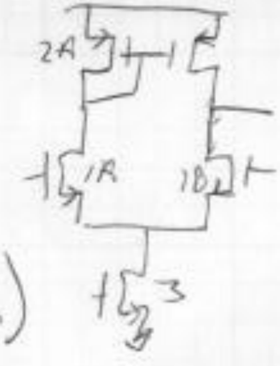
If $\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_3$ then $I_{D4} = I_{D5} \approx I_{D3}$

M4 must carry the same current as M2A+B

so make $\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_{2A} + \left(\frac{W}{L}\right)_{2B} = 2\left(\frac{W}{L}\right)_{2A}$

If $\left(\frac{W}{L}\right)_5 = \alpha\left(\frac{W}{L}\right)_3$ $\quad \left(\frac{W}{L}\right)_4 = 2\alpha\left(\frac{W}{L}\right)_{2A}$

Input range,



$V_{icm,min} \approx V_{ov3} + V_{tn} + V_{ov1}$

$V_{icm,max} = V_{D2A} + V_{tn}$

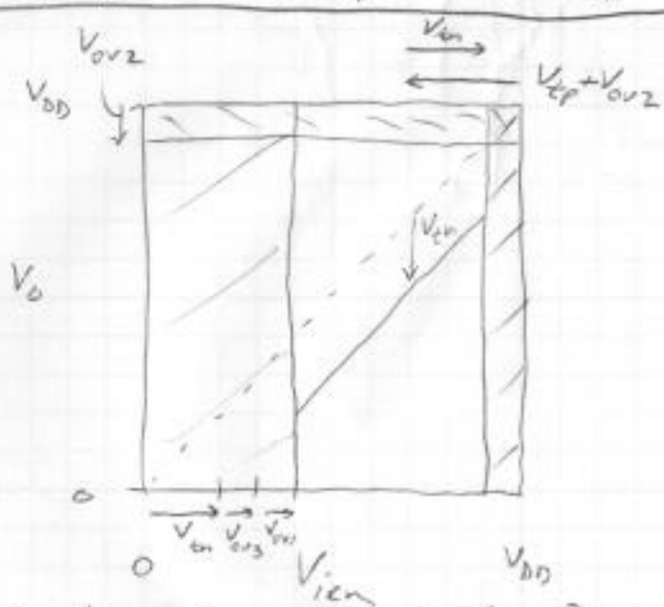
$\approx \left(V_{DD} - |V_{tp} + V_{ov2}| + V_{tn}\right)$

$\approx V_{DD} - |V_{ov2}|$

since $V_{tn} \approx -V_{tp}$ typically

$V_{o,max} = V_{DD} - |V_{ov2}|$

$V_{o,min} = V_{i,cm} - V_{tn}$



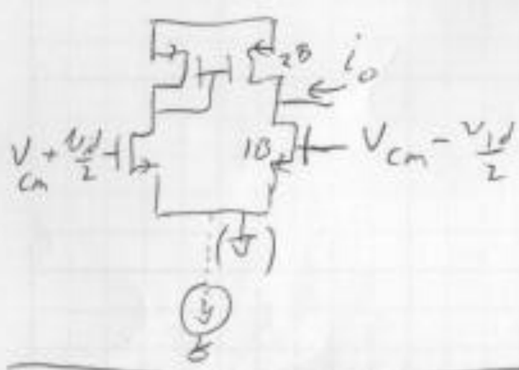
How does 2-stage change this picture?

$V_{O,min} = V_{ov5}$

Differential gain

common ~~false~~ assumption gives the right answer & some intuition.

Assume (incorrectly) that the tail is virtual ground

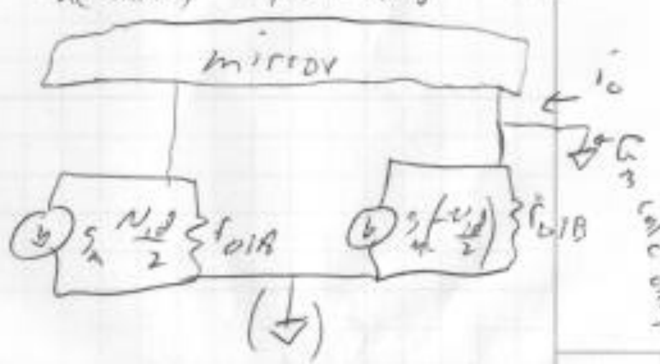


$$G_m = \frac{i_o}{v_{id}}\bigg|_{v_o = 0}$$

$$R_o = \frac{v_o}{i_o}\bigg|_{v_{id} = 0}$$

$$R_o = r_{o1B} \| r_{o2B} = \frac{1}{\lambda_n (I_{tail}/2)} \| \frac{1}{\lambda_p (I_{tail}/2)} = \frac{1}{\lambda I_{tail}}$$

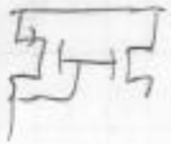
G_m

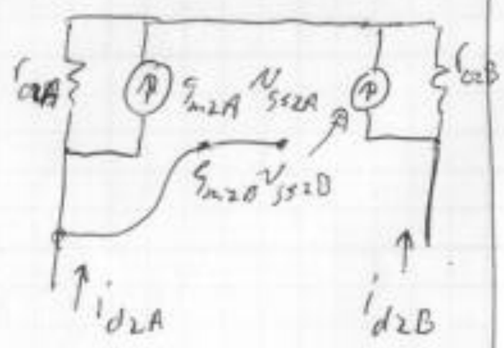


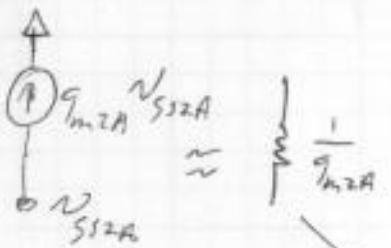
$$i_o = i_{d1B} + i_{d2B}$$

$$i_{d1B} = g_m\left(\frac{-v_{id}}{2}\right) = -\frac{g_{m1}}{2} v_{id}$$

i_{d2B}







$$i_{d2B} = g_{m2B} v_{ss2B}$$

mirror

$$= g_{m2B} v_{ss2A}$$

$$\approx g_{m2B}\left(i_{d2A} \frac{1}{g_{m2A}}\right)$$

$$= i_{d2A}$$

$$i_{d2A} = -i_{d1A} = -g_m \frac{v_{id}}{2}$$

$$i_o = i_{d1B} + i_{d2B} = -\frac{g_{m1B}}{2} v_{id} - \frac{g_{m1A}}{2} v_{id}$$

$$= -g_{m1} v_{id}$$

$$A_{v1} = -G_m R_o = +g_{m1}(r_{o1} \| r_{o2}) = \frac{2(I_{tail}/2)}{V_{ov}} \frac{1}{\lambda I_{tail}}$$

$$= \frac{1}{\lambda V_{ov}} = \frac{V_A}{V_{ov}}$$