

**PROBLEM SET #10**

Issued: Tuesday, April 14, 2009

Due: Tuesday, April 28, 2009, 8:00 p.m. in the EE 140 homework box in 240 Cory

1. This problem concerns the CMOS operational amplifier shown in Fig. PS10-1.

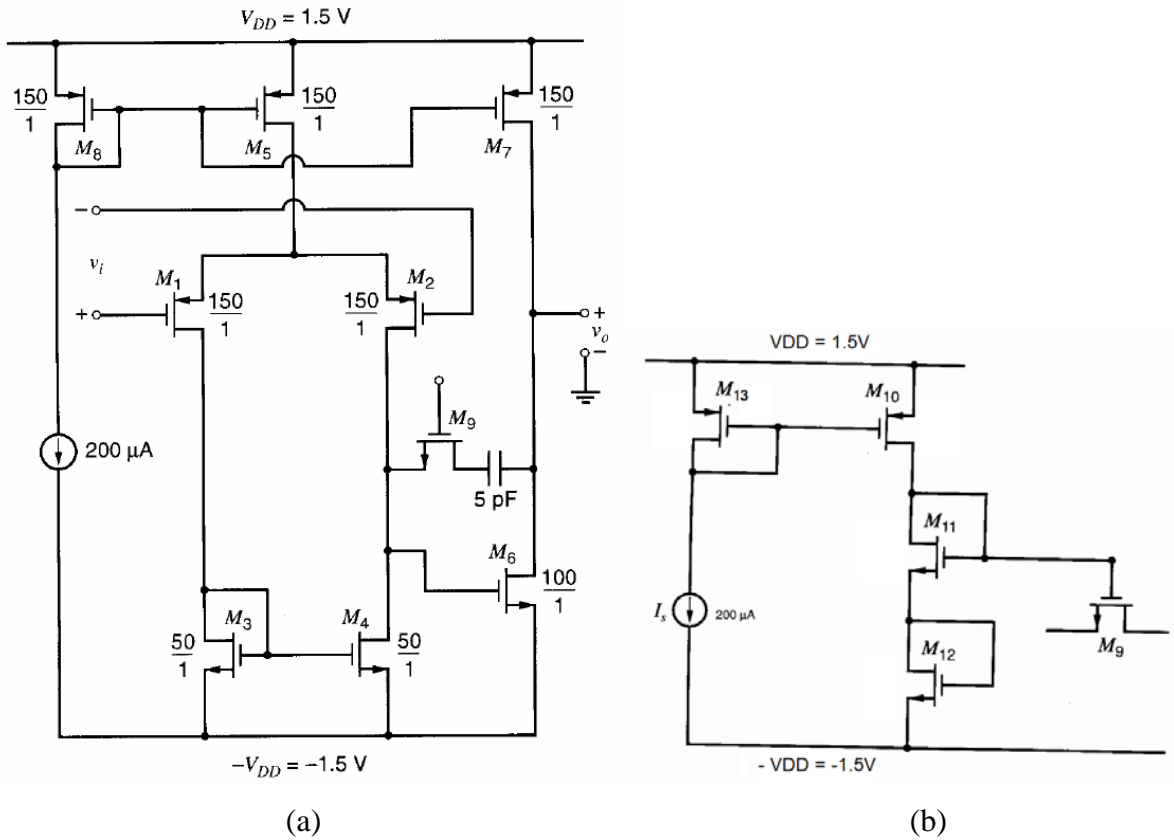


Figure PS10-1

Variable	NMOS	PMOS	Unit
$X_d$	0.1	0.1	$\mu\text{m}$
$dX_d/dV_{ds}$	0.02	0.04	$\mu\text{m}/\text{V}$
$t_{ox}$	80	80	$\text{\AA}$
$\mu$	450	150	$\text{cm}^2/\text{V}\cdot\text{s}$
$V_T$	0.7	0.7	V
$\gamma$	0	0	$\text{V}^{1/2}$

Table PS10-1

(a) Calculate the open-loop voltage gain, unity-gain bandwidth, and slew rate, for the circuit in Fig. PS10-1(a). Use the parameters of Table PS10-1. Assume that the gate of  $M_9$  is connected to the positive power supply and that the  $W/L$  ratio of  $M_9$  has been chosen to cancel the right half-plane zero. Compare your results with a SPICE simulation.

- (b) If the circuit of Fig. PS10-1(b) is used to generate the voltage to be applied to the gate of  $M_9$  in Fig. PS10-1(a), calculate the  $W/L$  ratio of  $M_9$  required to move the right-half plane zero to infinity. Let  $V_{DD} = 1.5$  V and  $I_s = 200$   $\mu$ A. Use  $L = 1$   $\mu$ m for all transistors,  $W_{I3} = W_{I0} = 150$   $\mu$ m, and  $W_{I1} = W_{I2} = 100$   $\mu$ m. Use Table PS10-1 for other parameters.
- (c) Assuming that the zero has been moved to infinity, determine the maximum load capacitance that can be attached directly to the output of the circuit of Fig PS10-1(a) and still maintain a phase margin of  $45^\circ$ . Neglect all higher order poles except any due to the load capacitance. Use the value of  $W/L$  ratio obtained in part (b) for  $M_9$  with the bias circuit of Fig. PS10-1(b). Ignore junction capacitance for all transistors. Use Table PS10-1 for other parameters.

2. The amplifier  $a(s)$  has one real negative pole and is configured as an inverting feedback amplifier as shown in Fig. PS10-2.
- (a) Calculate the DC gain of the amplifier  $a(s)$  such that the static gain error of the feedback amplifier is 0.05%.
- (b) Calculate the pole location such that the settling time is 10ns for 0.05% accuracy.
- (c) If the open loop amplifier has a second pole that produces 60% phase margin for the feedback configuration in Figure 2, what is the new settling time? For this part you can use either analytical methods or numerical simulations.

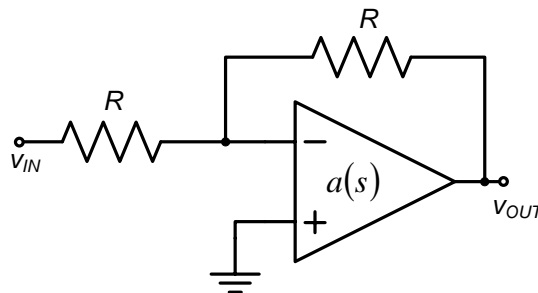


Figure PS10-2

3. Razavi, Chapter 10: Problem 10.9.
4. Razavi, Chapter 10: Problem 10.10.
5. Razavi, Chapter 9: Problem 9.3.