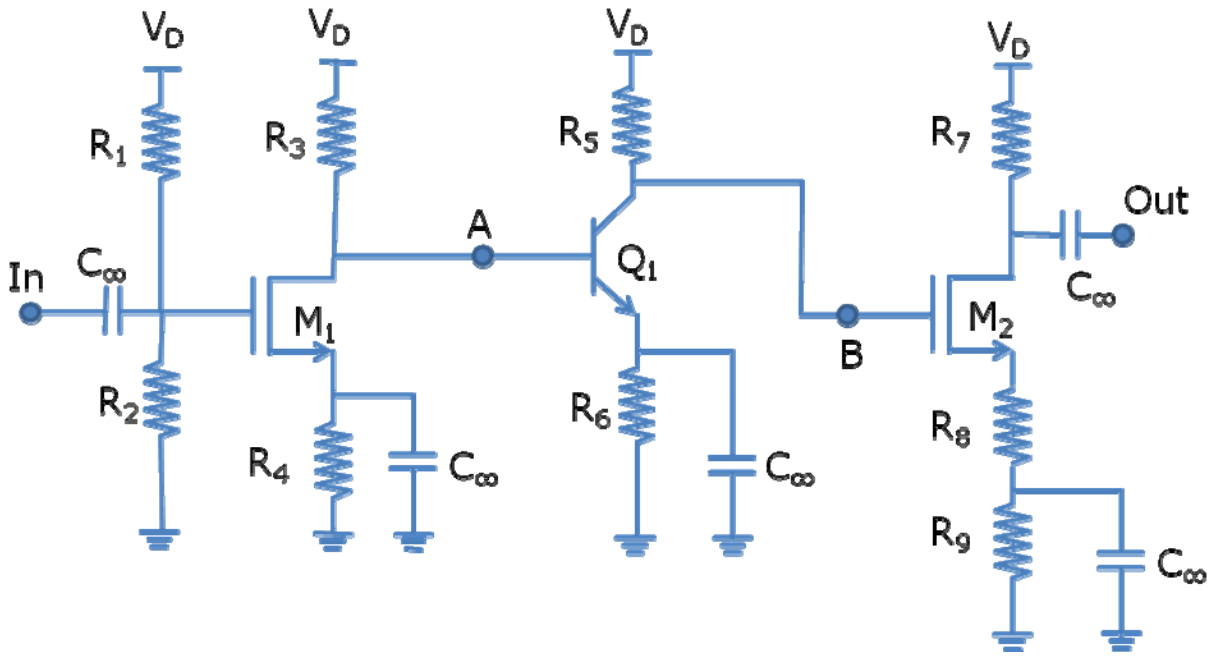
PROBLEM SET #3

Issued: Tuesday, Feb.10, 2009

Due: Tuesday, Feb.17, 2009, 6:00 p.m. in the EE 140 homework box in 240 Cory

1. For the circuit below with the given parameters, answer the questions that follow.



Parameters:

$R_1 = 3.5\ \text{k}\Omega$ $R_2 = 1.5\ \text{k}\Omega$ $R_3 = 2.5\ \text{k}\Omega$ $R_4 = 0.7\ \text{k}\Omega$ $R_5 = 2.5\ \text{k}\Omega$

$R_6 = 1.8\ \text{k}\Omega$ $R_7 = 2\ \text{k}\Omega$ $R_8 = 0.25\ \text{k}\Omega$ $R_9 = 1.4\ \text{k}\Omega$

$V_D = 5\ \text{V}$ $C_\infty = 1\ \mu\text{F}$

For BJT devices:

$V_{BE(on)} = 0.7\ \text{V}$ $V_{CE(sat)} = 0.2\ \text{V}$ $V_{BE(sat)} = 0.8\ \text{V}$ $r_o = \infty$

$f_t = 10\ \text{GHz}$ $C_\mu = 0.2\ \text{pF}$ $\beta = 100$

Consider only C_π and C_μ for high frequency calculations.

For MOS devices:

$V_{th} = 0.6\text{V}$ $(W/L)_{M1} = 380$ $(W/L)_{M2} = 242$ $L_{1,2} = 1\ \mu\text{m}$

$r_o = \infty$ $C_{ox} = 3.84\ 10^{-3}\ \text{F/m}^2$ $\mu_n C_{ox} = 133.3\ \mu\text{A/V}^2$

$C_{ov} = 1\ \text{fF} / \mu\text{m}$ (overlap capacitance per unit width)

Consider only C_{GS} and C_{GD} as device parasitic capacitances for high frequency calculations.

Hint: "Miller effect" can help you to locate high frequency time-constants at the circuit nodes.

(a) Determine the DC operating point of each transistor, i.e. specify operating region, DC current through drain (or collector), and DC voltages at drain (or collector), gate (or base), source (or emitter).

(b) Find an expressions and numerical values for the following parameters:

i. input impedance seen looking into terminal "In"

ii. output impedance seen looking into terminal "Out".

iii. midband voltage gain from "In" to "Out".

(c) Determine the high 3dB cut-off frequency, f_H.

(d) Determine the low 3dB cut-off frequency, f_L.

(e) Draw a Bode plot for the overall gain of the circuit. Include labels for important points and slopes.

2. For the CS-CD amplifier in Figure PS3.2, V_{DD}=5V, R_S=1kΩ, R_1=5kΩ, R_D=4kΩ, R_B=0.8kΩ, R_L=50Ω, C_1=10μF, C_2=10μF. Calculate R_2, W_1, and W_2 such that the overdrive voltages of both M_1 and M_2 are 250mV and the voltage at the point A is equal to 2V when no input signal is applied. Calculate the following:

(a) input and output impedance

(b) midband voltage gain

(c) low and high frequency pole(s) of the amplifier

All channel lengths are 0.5μm. All transistor bodies are connected to their respective sources. V_{th0}=0.75V, C_{ox}=15fF/μm^2, $\mu_n C_{ox}$=50μA/V^2, λ=0, C_{ov}=0.75fF/μm. Ignore drain-to-bulk and source-to-bulk capacitances.

Note: Overdrive voltage is defined as $V_{ov}=V_{gs}-V_T$.

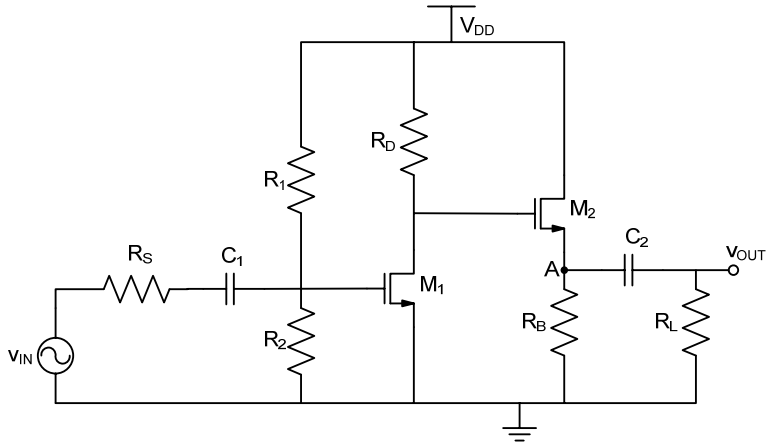


Figure PS3.2

3. Part (b) of Problem 4 in Problem Set #2 (which was deferred to this problem set).

4. For the common gate amplifier in Figure PS3.3, V_{DD}=3V, R_S=75Ω, R_L=1kΩ, C_1= 1μF, $C_2 \to \infty$, $C_3 \to \infty$. Assume all transistor channel lengths are 0.5μm. Answer the following questions.

(a) Calculate R_B and W such that the quiescent point output voltage is 2V and all transistors work in saturation for 1V<v_{OUT}<3V.

(b) What is the midband gain of the amplifier?

(c) Estimate both low and high frequency poles of the transfer function.

(d) Sketch the bode plot of the transfer function. Clearly mark all important points and slopes.

Use MOS parameters given in Table 2.1 in Razavi's textbook. Source/drain areas are 1.25μm × channel width, and are shared when possible. Single finger transistors are used in this design. All transistors are built on a single substrate connected to the ground.

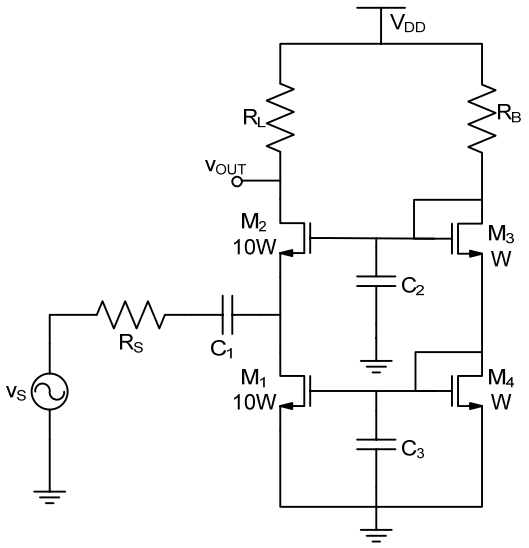


Figure PS3.3