PROBLEM SET #5

Issued: Tuesday, Feb. 24, 2009

Due: Tuesday, March 3, 2009, 6:00 p.m. in the EE 140 homework box in 240 Cory

1. Razavi, Chapter 5: Problem 5.2.

2. Design the Widlar current source shown in Figure PS5.2 to produces 5 μA output current. Use identical transistors, V_{CC} = 30V, and R_1 = 30 kΩ. Find the output resistance.

BJT Parameters: β = 200, V_A = 130 V, $V_{BE,ON}$ = 0.7 V

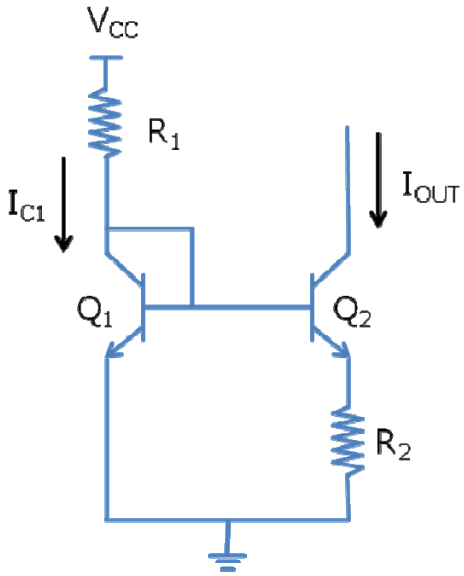

Figure PS5.2

3. This problem concerns the simple MOS current mirror shown in Figure PS5.3a.

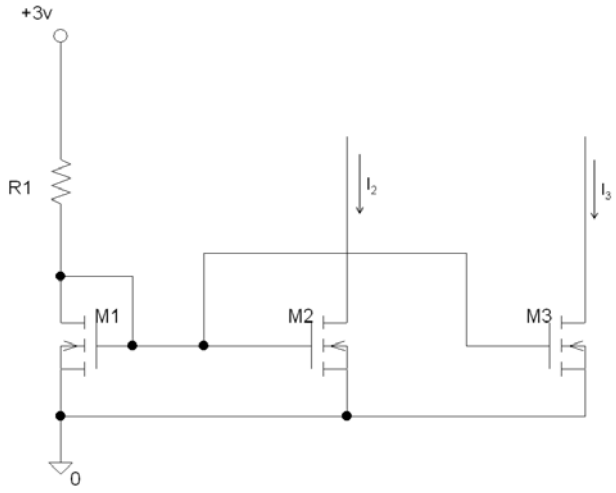

Figure PS5.3a

(a) Design the current mirror such that all of the following is satisfied:

i. The currents I_2=0.5mA and I_3=2mA (approximately).

ii. The minimum output voltage for which M_2 and M_3 work as current sources is 200mV.

iii. The output currents change less than 1% for a change in output voltage of 1V.

iv. All transistors should have the same channel length.

You are to minimize the total circuit area which is approximately given by

$$A = \sum_{i=1}^{3} W_i L_i + \beta R_1$$

The parameter λ can be calculated as $\lambda = \frac{\alpha}{L}$. α and β are constants.

$$\alpha = 0.02\frac{\mu m}{V},\quad \beta = 0.2\frac{\mu m^2}{\Omega},\quad C_{ox} = 5\frac{fF}{\mu m^2},\quad \mu_n = 450\frac{cm^2}{Vs},\quad V_{th0} = 0.6V$$

(b) A layout designer used long and narrow wires to connect sources of M_1, M_2, and M_3, which resulted in small parasitic resistances R_p=2Ω, as shown in Figure PS5.3b. What are the new values of I_2 and I_3? You can use numerical methods if needed.

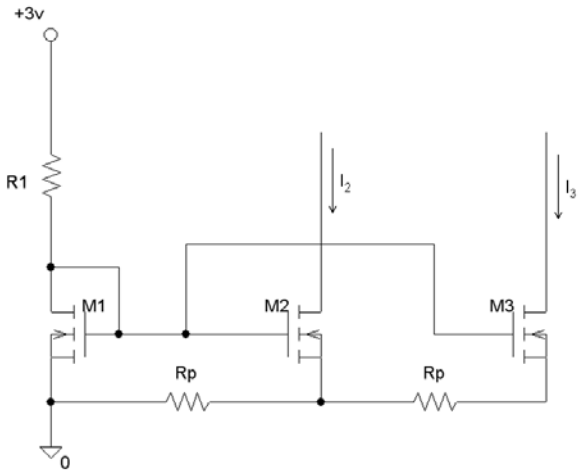

Figure PS5.3b

4. Razavi, Chapter 5: Problem 5.6.

5. Design the circuit shown in Figure PS5.5 to meet the following constraints:

(a) Transistor M_2 operates in the saturated region for values of V_{OUT} to within 0.2 V of ground.

(b) The output current must be 50 μA.

(c) The output current must change less than 0.02% for a change in output voltage of 1 V.

You are to minimize the total device area within the given constraints. Here the device area will be taken to be the total gate area (W X L product). Ignore the body effect for simplicity.

Make all devices identical except M_4. Use SPICE to check your design and also to plot the I_{OUT}-V_{OUT} characteristic for V_{OUT} from 0 to 3 V. Use the following process parameters: t_{ox}=8 nm, μ_n=450 cm^2/VS, L_d=0.09 μm, dX_d/dV_{DS}=0.02 μm/V (channel length modulation parameter, use it to get λ).

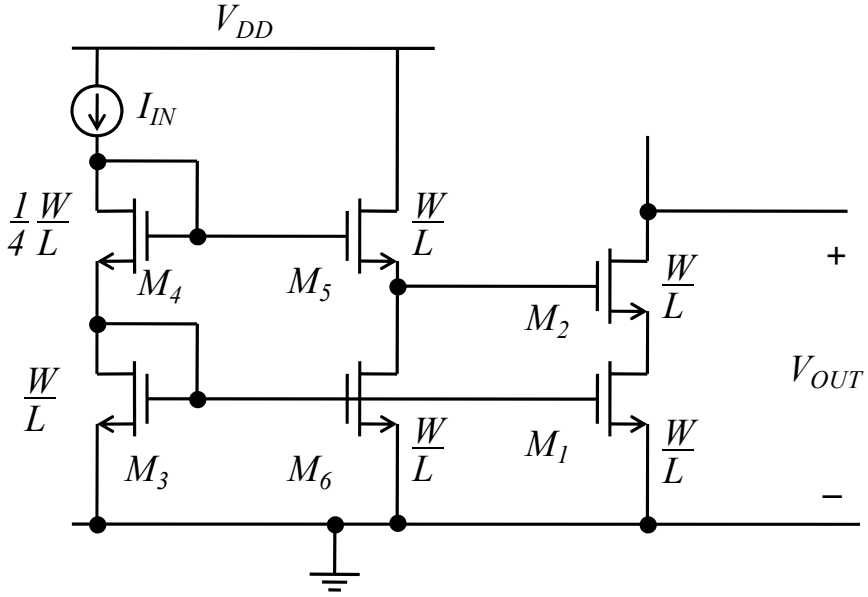

Figure PS5.5