PROBLEM SET #6

Issued: Tuesday, March 3, 2009

Due: Tuesday, March 10, 2009, **5:00 p.m.** in the EE 140 homework box in 240 Cory

1. For the high-swing cascode mirror shown in Figure PS6-1 answer the following questions:

(a) Calculate W such that the minimum output voltage for which both M_1 and M_2 are in saturation is 0.5V. Assume that M_3-M_5 can provide appropriate gate biases for M_1 and M_2.

(b) Calculate W_5 in order to achieve the minimum output voltage calculated in (a).

(c) Briefly explain the function of M_4.

(d) What is the output resistance of this current source?

(e) What is the change in I_{OUT} for ΔV_{OUT}=1V?

(f) What is the resistance seen by the ideal current source I_{IN} that biases M_3 and M_4?

(g) Calculate input voltages V_{IN1} and V_{IN2}.

(h) Replace transistors M_5 and M_6 with one diode connected device. What is the W of the new device?

$$I_{IN}=100\mu A,\quad L=1\mu m\quad C_{ox}=5\frac{fF}{\mu m^2},\quad \mu_n=450\frac{cm^2}{Vs},\quad V_{th0}=0.6V,\quad \lambda=0.02V^{-1},\quad \gamma=0$$

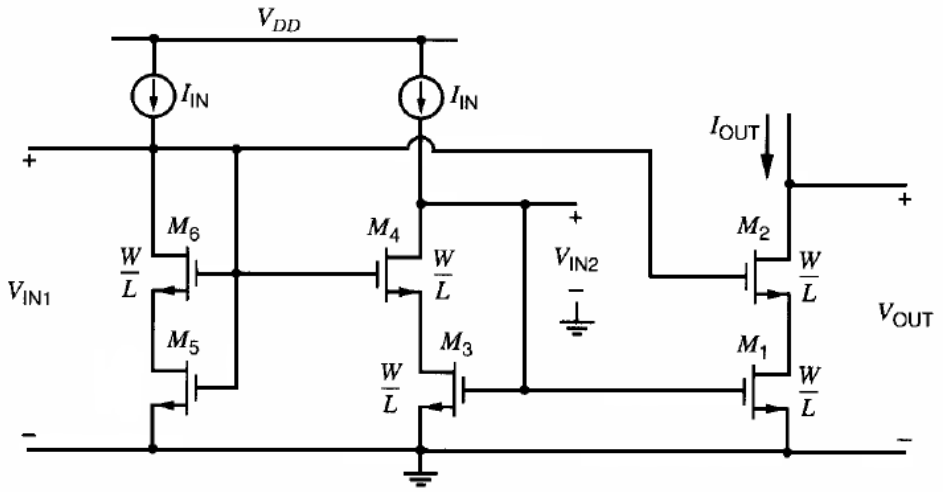

Figure PS6-1

2. Use half-circuit concepts to determine the differential-mode and common-mode gain of the circuit shown in Figure PS6-2. Neglect r_o, r_u and r_b. Then calculate the differential-mode and common mode input resistance.

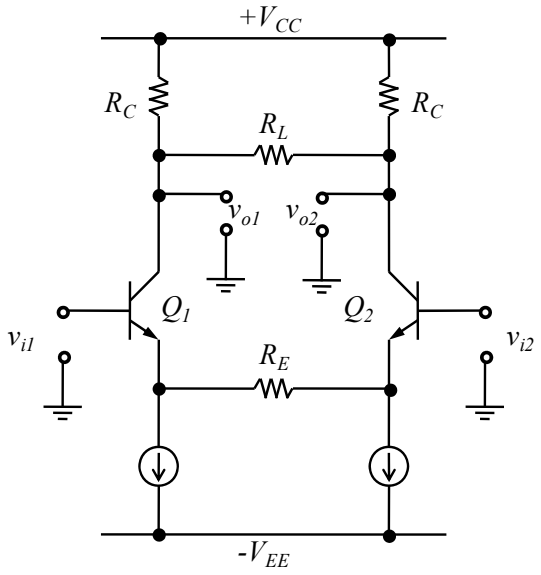

Figure PS6-2

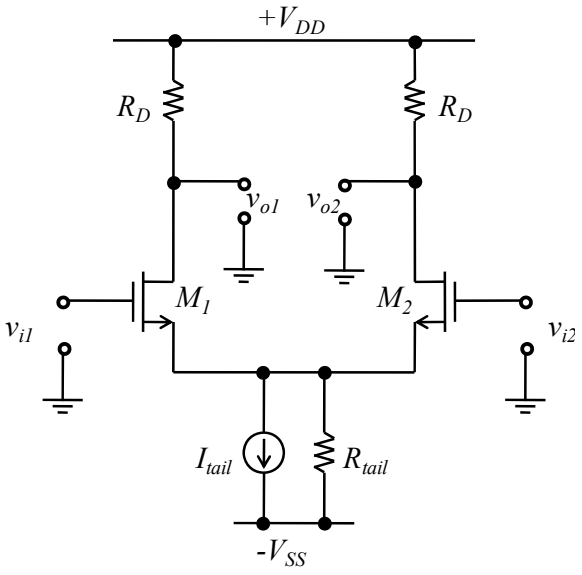

Figure PS6-3

3. Use half circuit analysis to determine (i) the differential-mode gain A_{dm}, (ii) the common-mode gain A_{cm}, (iii) the common-mode input to differential-mode output gain $A_{cm\text{-}dm}$, and (iv) the differential-mode input to common-mode output gain $A_{dm\text{-}cm}$ for a resistively loaded differential pair shown in Figure PS6-3 with mismatched resistive loads, R_1 and R_2. Assume that R_1=10.1kΩ, R_2=9.9kΩ, also assume $r_{o1}=r_{o2}=\infty$, and R_{tail}=1MΩ. Use the following process parameters: t_{ox}=8 nm, μ_n=450 cm^2/VS, L_d=0.09 μm, W=10um, L=1um. Then calculate the input offset voltage assuming a W/L mismatch of 2 percent besides the resistive load mismatch. Ignore the difference of the device threshold in your offset calculation.

4. This problem concerns the actively loaded MOS amplifier shown in Figure PS6-4.

(a) Design the amplifier to achieve a differential small signal gain of 200. Bias M_1 and M_2 with 100μA of current each. The maximum output swing should be 2V peak-to-peak. Do not use overdrive voltages lower than 150mV. Choose W_5 and W_6 so that the bias currents of M_5 and M_6 are exactly the same at the quiescent point. Use the smallest channel lengths that satisfy the gain requirements. All transistors should have the same channel lengths.

(b) If the desired output voltage at the quiescent point is in the middle of output signal range, what is the systematic input referred voltage offset of this amplifier?

(c) Due to manufacturing imperfections threshold voltages, channel widths and channel lengths can differ from designed by ΔV_{th}, ΔW, ΔL, where $|\Delta V_{th}| < 10mV$, $|\Delta W| < 5nm$, $|\Delta L| < 5nm$. What is the worst case input referred voltage offset due to mismatches?

$$V_{DD} = 1.8V,\ V_{SS} = -1.8V,\ V_{th0,n} = V_{th0,p} = 0.5V,\ \alpha_N = \frac{dX_d}{dV_{DS}} = 0.02\frac{\mu m}{V},\ \alpha_N = \frac{dX_d}{dV_{SD}} = 0.04\frac{\mu m}{V},$$

$$\mu_n C_{ox} = 250\frac{\mu A}{V^2},\ \mu_p C_{ox} = 100\frac{\mu A}{V^2},\ \gamma = 0,\ L_d = 0$$

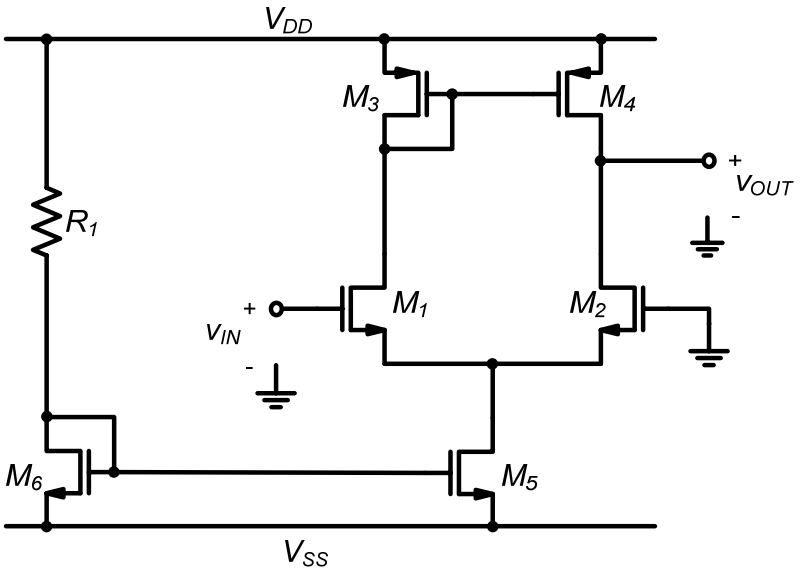

Figure PS6-4