PROBLEM SET #8

Issued: Tuesday, March 31, 2009

Due: Tuesday, April 7, 2009, **8:00 p.m.** in the EE 140 homework box in 240 Cory

1. This problem concerns the class B output stage shown in Figure PS8-1(a). The input signal is $v_{IN} = V_m \sin(2\pi f_{in} t)$.

(a) If the load is resistive $Z_L = R$ sketch timing diagrams of the output voltage $v_{OUT}(t)$, the load current $i_L(t)$, and collector currents $i_{C1}(t)$ and $i_{C2}(t)$.

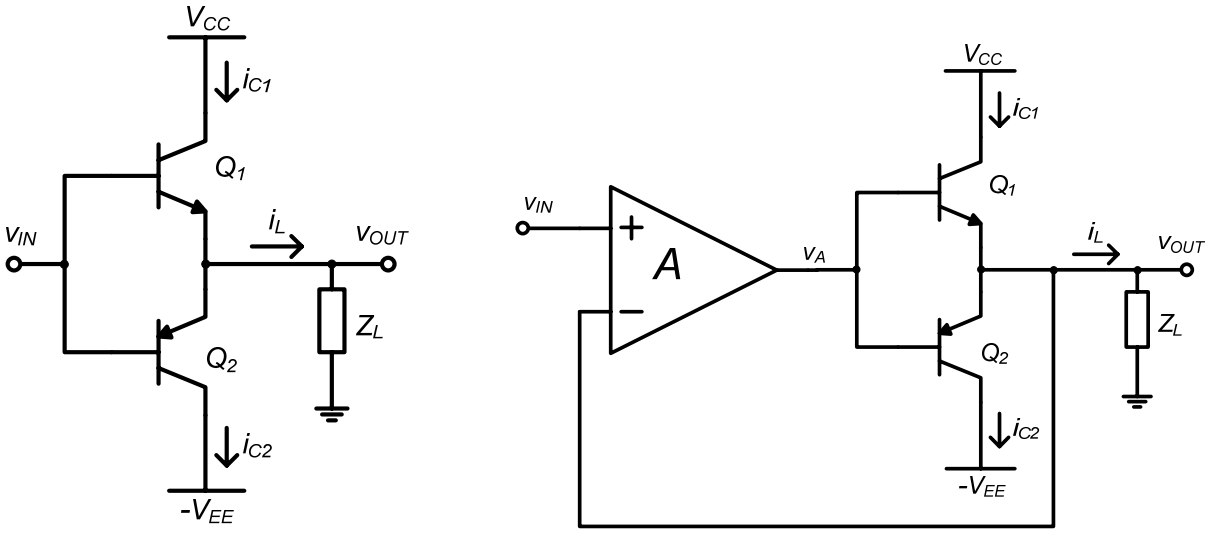
(b) Repeat **(a)** if the load is capacitive $Z_L = \dfrac{1}{j\omega C}$.

(c) The output stage is connected in a feedback loop as shown in Figure PS8-1(b). Sketch timing diagrams of $v_{OUT}(t), i_L(t), i_{C1}(t), i_{C2}(t)$, and $v_A(t)$ if $Z_L = R$. Assume amplifier *A* is ideal.

(d) Repeat **(c)** if $Z_L = \dfrac{1}{j\omega C}$.

Draw only one period in steady state. Clearly mark all important points in your diagrams.

$$V_m = 9V,\ f_{in} = 1kHz,\ C = 100\,pF,\ R = 500\Omega,\ |V_{BE,on}| = 0.7V,\ V_{CC} = V_{EE} = 10V.$$



(a) (b)

Figure PS8-1

2. The slew rate of the circuit in Fig. PS8-2 is to be increased by using two 10 kΩ resistors placed at the emitters of Q_1 and Q_2. If the same unity-gain frequency is to be achieved, calculate the new value of compensation capacitor required and the improvement in slew rate.

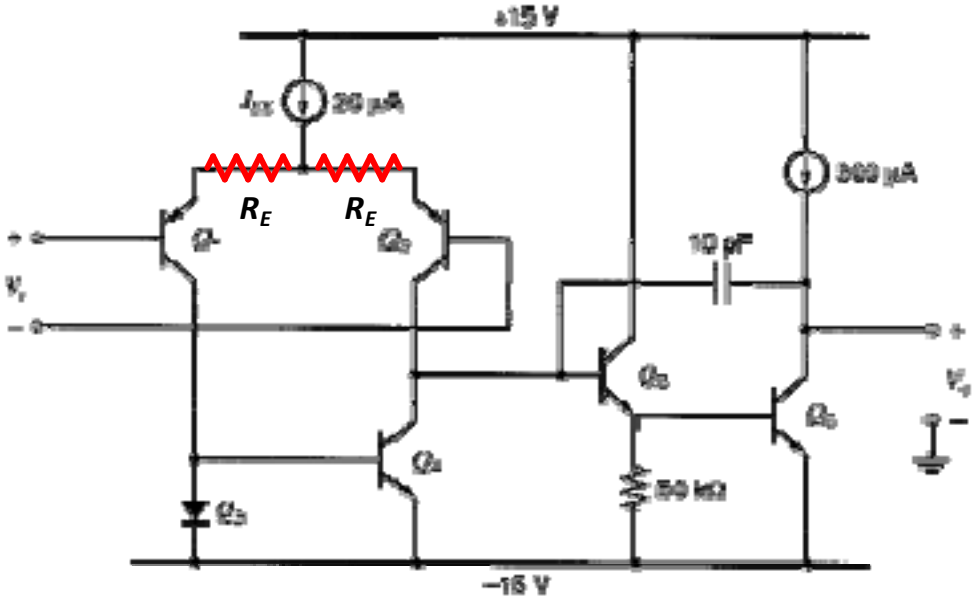


Figure PS8-1

3. Razavi, Chapter 9: Problem 9.19.

4. Razavi, Chapter 9: Problem 9.20.