Experiment 2: Discrete BJT Op-Amps (Part I)

This is a three-week laboratory. You are required to write only one lab report for all parts of this experiment.

1.0. INTRODUCTION

In this lab, we will introduce and study the properties of a few circuit blocks commonly used to build operational amplifiers. Because we are limited to using discrete components, we will not be able to construct a complete op-amp. This will be done in the op-amp design project later in the semester. In this lab, however, we will ask you to analyze and design circuits commonly used to make integrated circuit operational amplifiers, and you will use these circuits to build a differential amplifier with both resistive and current mirror biasing. Although built with discrete devices, this op-amp uses a classical topology common to most commercial op-amps including the well-known 741.

The operation of these circuits will depend on the use of matched transistors. The CA3083 is a matched NPN transistor array built on a single integrated substrate. To ensure that the transistors are properly isolated, you must connect pin 5 of the array to the most negative point of the circuit (-6 volts). Data sheets for the CA3083, and discrete npn and pnp transistors needed in this lab are attached.

In this lab more than any other so far, neatness counts. Unless you build your circuits neatly, they will not operate. Trim your resistor leads if necessary.

Make sure that you record all the measurements that you make as you proceed, and include these measurements in your lab report.

2.0. MATERIALS REQUIRED

- CA3083 NPN Array
- 2 - 3904 Transistor
- 2 - 3906 Transistor
- Assorted Resistors and Capacitors

3.0. PROCEDURE

3.1 Differential Amplifier

Consider the following circuit:

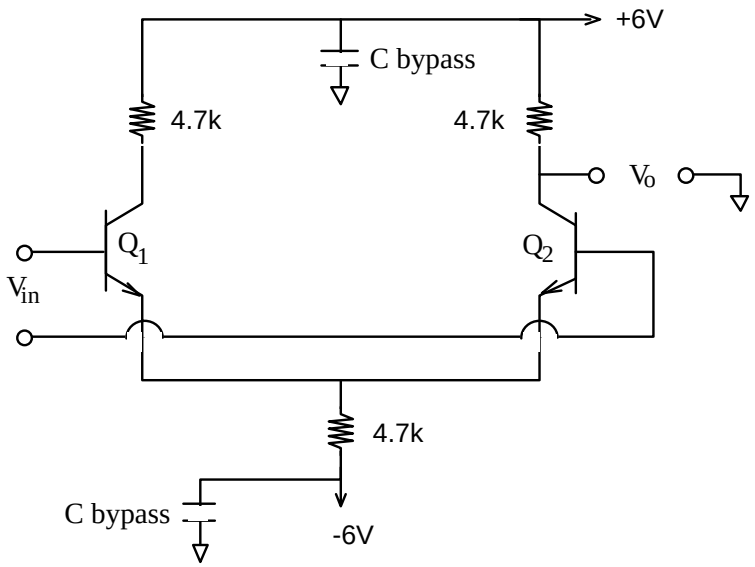


Figure 1

- Assuming that both bases are grounded, compute the expected values of IC1, IC2 and IE. Also calculate values for the differential and common mode gains of this amplifier.
- Using transistors 1 and 2 in the array, construct the circuit in Figure 1. Be sure to connect pin 5 to -6 volts. It is also a good idea to bypass both your power supplies with 100µF capacitors. This will help reduce any power supply noise.

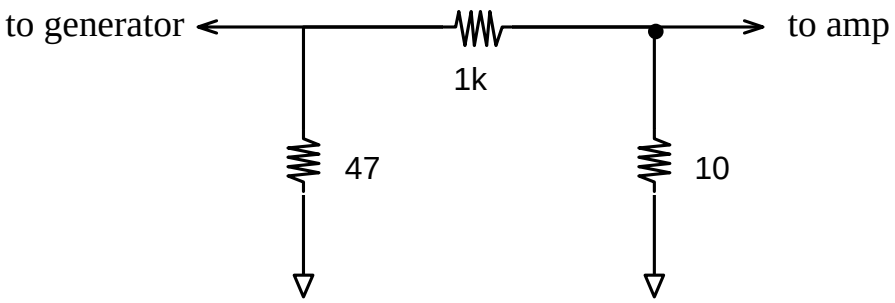


Figure 2

- With both bases grounded, measure the bias point of the circuit.
- Using one generator, measure the mid-band differential (note that the output of the amplifier is taken single-ended from only one collector) and common mode gains of the circuit. You may find that a resistive voltage divider such as the one pictured in Figure 2 is helpful in measuring the differential mode gain. Be careful when measuring the common mode gain, especially when measuring voltages less than 50 mV (remember that the common-mode voltage gain is smaller than 1). Sometimes voltages of this magnitude are severely corrupted by ground currents from large signals on the board (such as the input to the amplifier) while making a common mode gain measurement). In any case, you should not use the input divider for common mode measurements, because your common-mode signal will likely be a large signal.

After making these measurements, do not disconnect your circuit. You will need it later.

3.2. Simple Current Mirrors

The circuits depicted in Figure 3 are the simple and the Widlar current mirrors. Fig. 3a shows the simple current mirror circuit. Its operation is simple and has been discussed in the lecture. Note that Vbe is identical for both transistors. Neglecting base current, IC3 = (12-Vbe3-Vbe3b)/R. Since Vbe3 = Vbe4, assuming that VC4 is large enough to keep Q4 in the active region, IC4 = IC3. More transistors can be connected in parallel to Q4 and (neglecting base currents) their IC will be identical to that of Q3. Thus, Q3's collector current is "mirrored" by Q4.

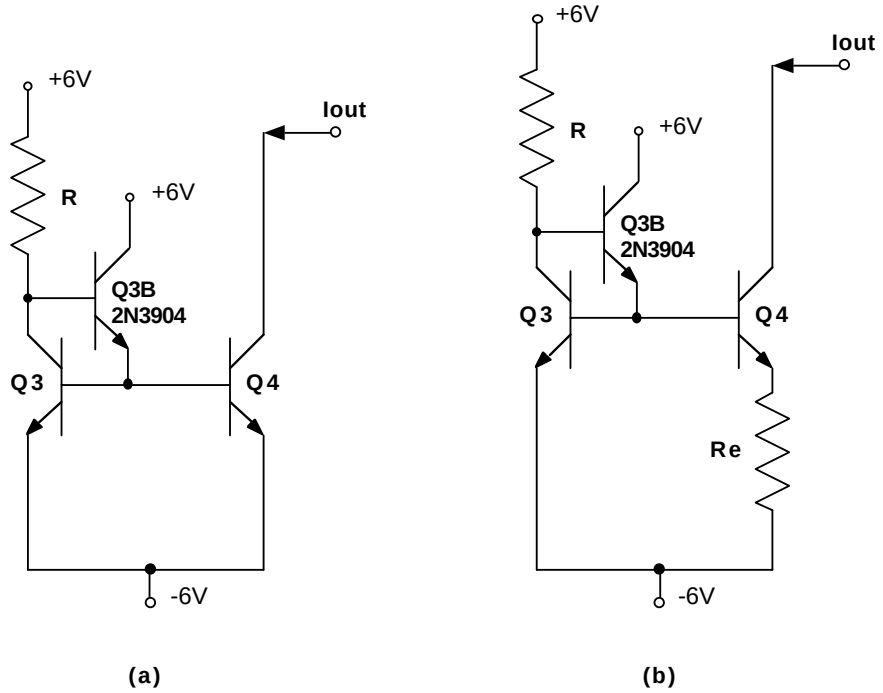


Figure 3

Current sources are often used for biasing in integrated circuits since large value resistors require large areas to fabricate.

1- Construct a simple current mirror circuit:

- Assuming $\beta = 150$, Vbe = .7V, and neglecting the Early effect, select a value of R (standard values only) to yield an output current of about 1 mA for the simple current mirror in Fig. 3a.
- Using transistors 3 and 4 in the array, construct the current mirror you designed above.
- Measure Iout for Vout = 0 V and +6 V. Using this data, form an estimate of the Early Voltage. Remember this is supposed to be a current source, which means it should have a high output resistance, Rout. To measure the output resistance you can connect different size load resistors to the output and see how the output current (voltage) changes as the load resistance changes (the other side of the load resistor should of course go to the +6V power supply. Also note that in order to minimize errors in your measurements, you should choose load resistor values that force the output voltage to change from about -5V to about +5V). Measure the output resistance of your circuit.

2- Construct a Widlar current mirror circuit.

- Design a Widlar current source that produces an output current of ≈1mA. Use the same parameters for the BJT as above. Use an emitter resistance value of Re=68Ω, and calculate the value of resistance R needed to produce the 1mA current. What is the reference current needed to produce the 1mA output current?
- Using transistors 3 and 4 in the array, construct the current mirror you designed above.
- Measure Iout for Vout = 0 V and +6 V. Using this data, form an estimate of the Early Voltage. Remember this circuit is a current source, which means it should have a high output resistance, Rout. To measure the output resistance you can connect different size load resistors to the output (the other side of the load resistor should of course go to the +6V power supply. Also note that in order to minimize errors in your measurements, you should choose load resistor values that force the output voltage to change from about -5V to about +5V) and see how the output current changes as the load resistance changes. Measure the output resistance of your circuit. Note the output resistance of this Widlar source should be higher than the standard current mirror. Compare the results obtained with these two sources.

3.3. Differential Pair Amplifier with Current Source Biasing

Replace Re in the differential amplifier built in Section 3.1 with the **Simple** current source constructed in Section 3.2. Your circuit should now look like Figure 4.

- Calculate and measure the bias point and the mid-band differential (note that the output of the amplifier is taken single-ended from only one collector) and common mode gains for the new differential amplifier. Compare your calculated and measured results.

LEAVE THIS CIRCUIT ON YOUR BREADBOARD AS YOU NEED TO USE IT IN NEXT WEEK'S LAB EXPERIMENT.

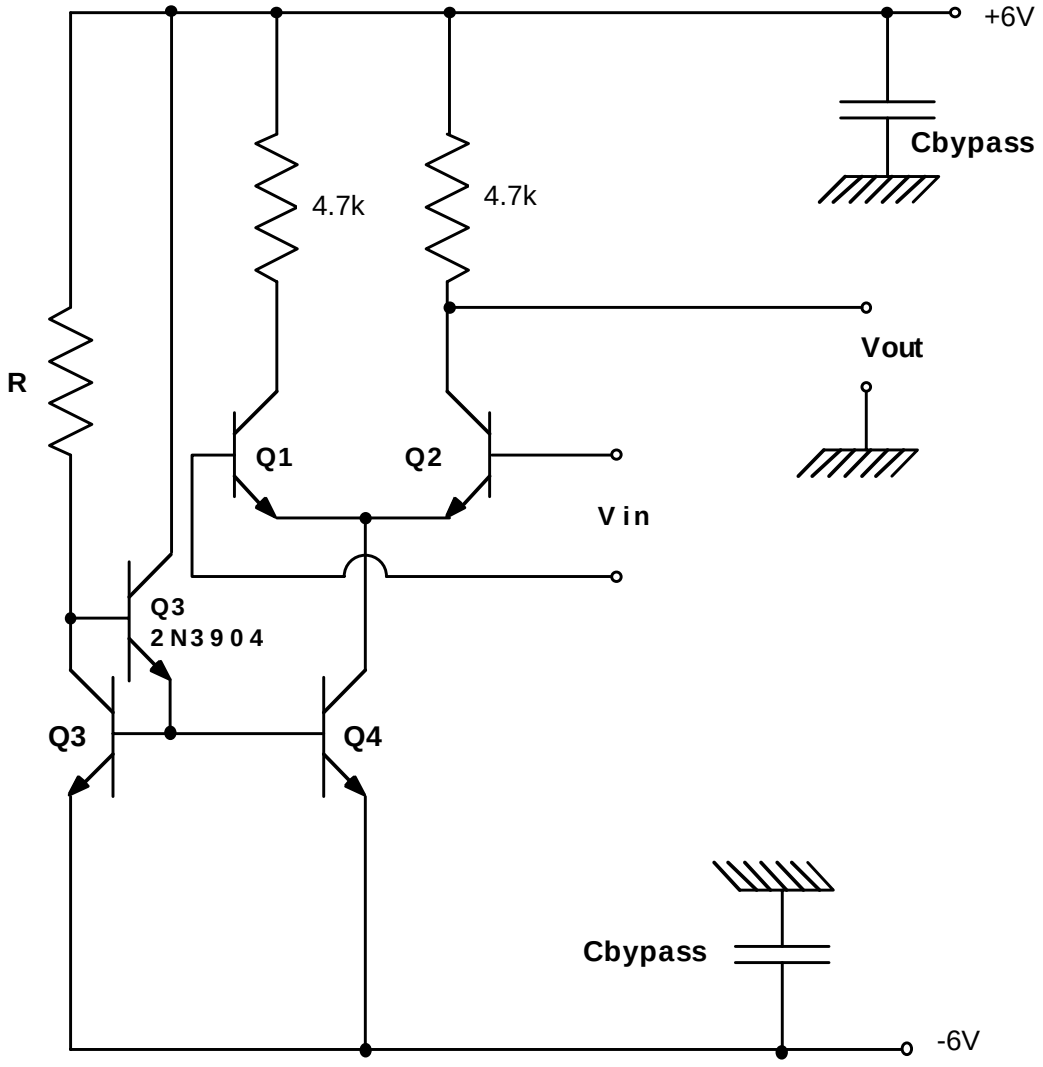


Figure 4

Experiment 2: Discrete BJT Op-Amps (Part II)

3.4. THE OP-AMP

In last week's lab experiment you designed current mirrors and built and tested the first stage of an operational amplifier, namely the input differential pair stage. As mentioned before, since we are using mostly discrete components, we have had to use resistive loads for the first stage. In this part of this laboratory you will build the second gain stage of the op-amp, but we will use an active load to illustrate the design of active loads in amplifier circuits.

Construct the circuit shown in Figure 5. Note that the first part of the circuit (i.e. the differential input stage) was built in your last week's lab. Use the same resistor values you had calculated and used last week. Note that transistor Q5 in this circuit is the number 5 transistor in the CA3083 transistor array, while transistor Q6 is a discrete pnp transistor (2N3906, for which data sheets are available). Also note that there are two compensation capacitors in this circuit, one is Cc (used in the Miller configuration), and the other is C, simply added from the output node to VCC (which is ac ground).

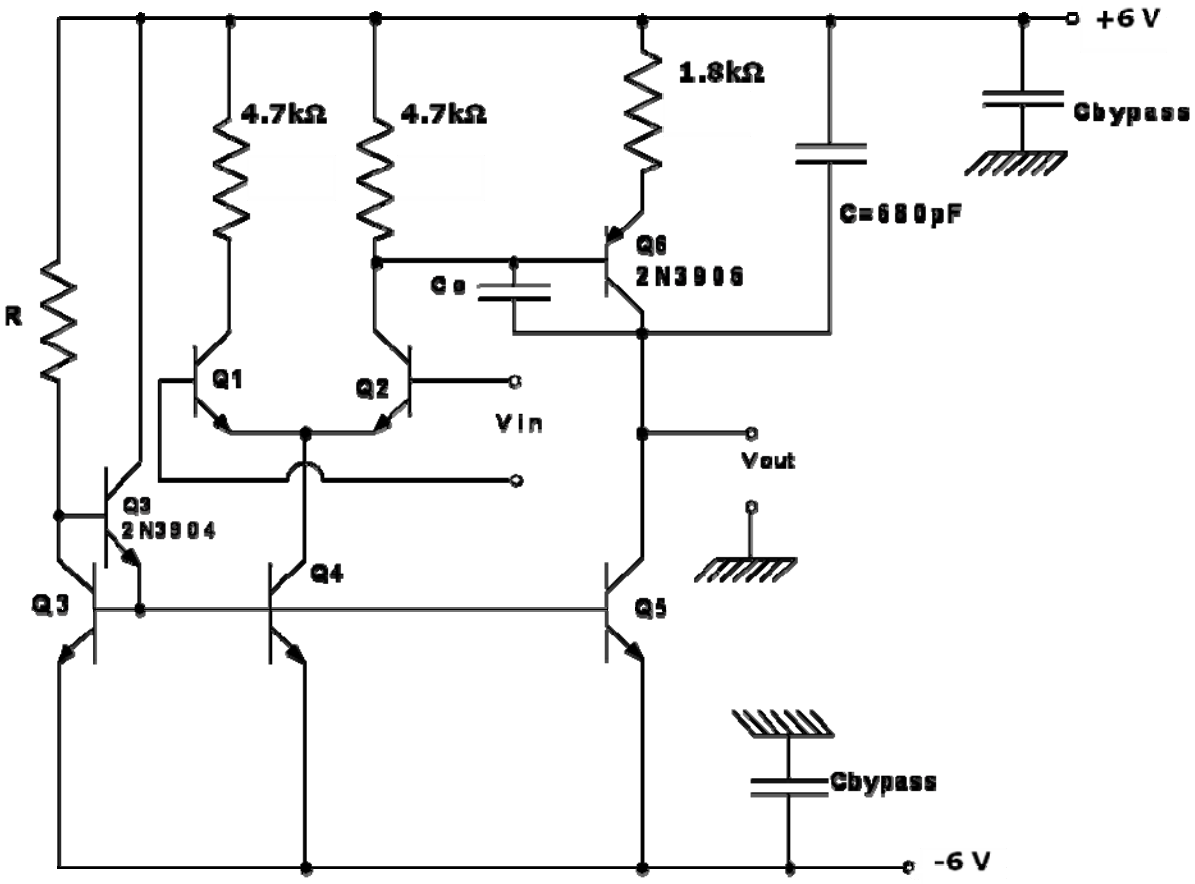


Figure 5

Transistors Q5 and Q6 together form the second gain stage of the amplifier, Q6 is the common-emitter amplifier transistor, while transistor Q5 acts as the active load for Q6. Note also that there is degeneracy added into the CE amplifier transistor Q6 (through the use of the 1.8kΩ resistor). As mentioned above, the circuit is compensated (that is the frequency response is stabilized) by adding the capacitor C=680pF to the output of the second gain stage. A second capacitor Cc is also shown attached to the circuit. This capacitor is added across the base and collector of transistor Q6 and utilizes the Miller effect. ***Note that you should not add both capacitors C and Cc to the circuit at the same time.*** First just add the 680pF capacitor C to the circuit and measure the following characteristics for the amplifier circuit:

a- Measure the dc transfer characteristics of the amplifier, Vo vs. Vin, which can be done either using a variable DC input source, or using the HP4145 parameter analyzer. This measurement can be done by simply measuring the DC output voltage of the amplifier as the input dc voltage is swept a particular range. Note that this amplifier is expected to have a large gain of a few thousand. Therefore, if the maximum output voltage range is to be from -6V to +6V (set by the supplies, although the actual output range will be much less than this), then the input voltage range should be from about -5mV to about +5mV. To change the DC input voltage, you can simply use the DC offset on the waveform generators. Of course you should pass the output of the generator through a simple attenuator network like the one used in last week's lab. It is also possible to measure the dc transfer characteristics using the HP 4145 parameter analyzer. Your TA will explain in detail how this can be done.

b- After measuring the transfer characteristics determine the offset voltage of the amplifier, and estimate its gain by calculating the slope of the Vo vs. Vin curve at the point where Vo=OV. Note that the slope of the dc transfer curve should be approximately equal to the ac gain that you will measure later.

c- Measure the differential and common-mode gains of the op-amp circuit, and its frequency response using the 680pF capacitor at the output. Note that the gain values can be measured the same way that was in last week's lab. However, now since the gain of the amplifier is very high you should try to apply a DC offset at the input so that the output DC voltage with no ac input applied is equal to about zero (the output DC voltage

should be measured by a voltmeter and not on the scope). Then you should apply your ac signal and measure the differential gain and the bandwidth. Make sure that you measure sufficient number of points so that you can plot the gain as a function of frequency and determine the upper cutoff frequency of the amplifier. You should then draw the Bode plot for the amplifier.

d- Note that the compensation capacitor C=680pF used for the op-amp is a fairly large capacitor. We can use the Miller technique and the Miller capacitance Cc in order to reduce the total amount of capacitance needed. We will ask you to estimate the value of the Miller capacitance needed to compensate this amplifier in next week's lab. For now do not use the Miller capacitance. If we had utilized the Miller capacitor Cc we could choose a much smaller value.

e- Measure the DC voltage at the collector of Q2 (base of Q6), V_{C2}, the voltage drop across the load resistor for the differential amplifier (which is simply 6-V_{C2}), the voltage at the emitter of Q6, V_{E6}, and the voltage drop across the emitter resistor of Q6, which is simply 6-V_{E6}.

After measuring the gain of this amplifier, you should calculate the approximate value of the overall voltage gain of this amplifier as a function of the DC voltages measured in part (e) above, and the Early voltages of the transistors, V_A. That is calculate the overall voltage gain A_{vd}, as a function of V_A's, $V_{C2,}V_{E6,}$ and VCC (VEE). Is this voltage gain dependent on the load resistors in the differential stage? Is the gain dependent on the emitter resistor of Q6? How can the differential gain of this amplifier be increased? You should discuss and provide answers to these questions in your lab report.

In the next part of this lab, we will ask you to complete the op-amp by adding the output stage and by adding the Miller compensation capacitor. You will also utilize your op-amp to build amplifier configurations (similar to those you build with the 741 op-amp), and to make additional measurements of op-amp characteristics.

Experiment 2: Discrete BJT Op-Amps (Part III)

This week you will complete the op-amp circuit by adding the last output stage to the circuit that you have been building during the past two weeks. In last week's lab experiment you completed the second gain stage and obtained data on the differential and common-mode gains of the op-amp without the output stage. This week you will continue to make measurements with all the circuit blocks included. As was mentioned before, this op-amp differs from the 741 op-amp in the design of its circuit blocks, but is very similar in the number of stages it has and in the overall topology. Therefore, it is a good experiment for illustrating some of the characteristics of op-amp circuits.

THE OP-AMP

Construct the circuit shown in Figure 6 by adding the class AB output stage to the amplifier circuit that you have already built in the previous two labs. Note that for the output stage you have to use two discrete bipolar transistors: a 2N3906 pnp and a 2N3904 npn transistor. The rest of the circuit is as before. Make sure that you check all your connections and your circuit board and eliminate any wiring mistakes or loose connections.

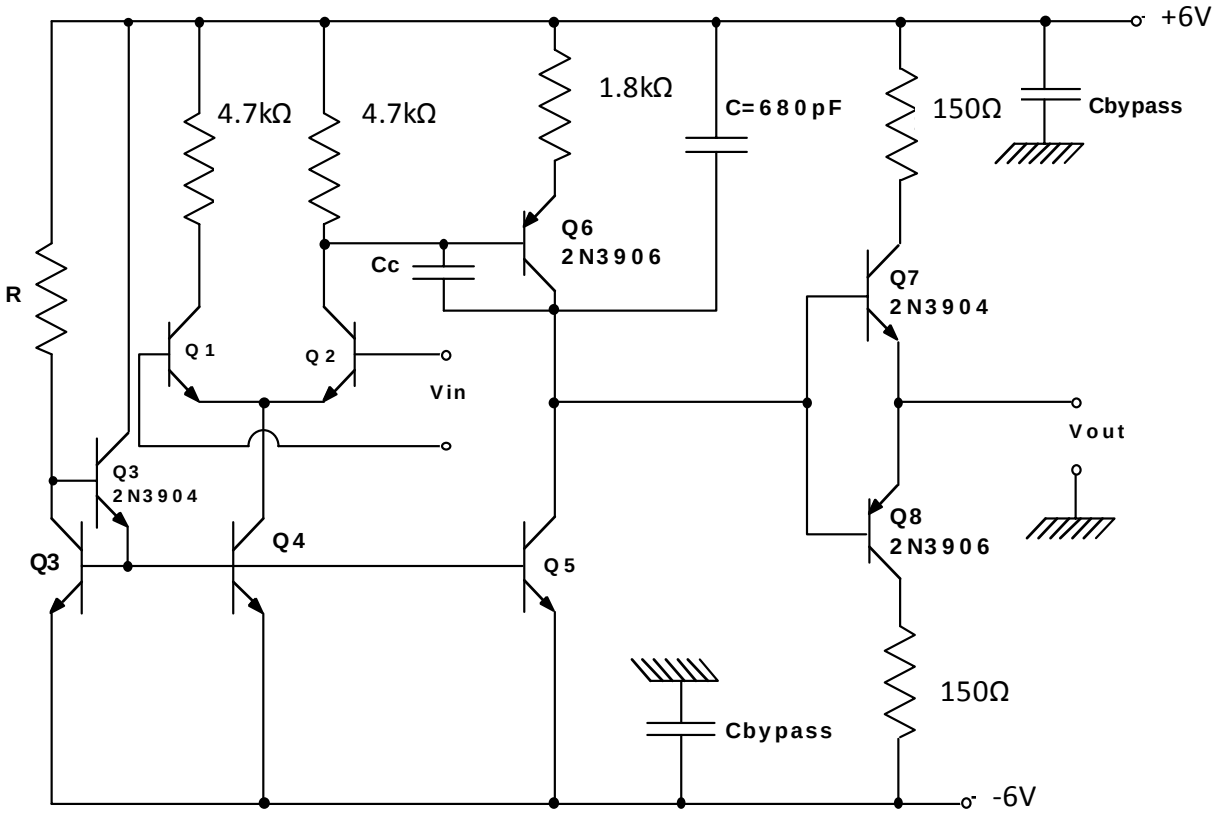


Figure 6: Circuit diagram for a complete discrete operational amplifier.

This circuit is a classical op-amp design with transistor Q5 and Q6 forming the second gain stage and transistors Q7 and Q8 forming the output stage. The circuit is compensated (that is the frequency response is stabilized) by adding capacitor C=680pF to the output of the second gain stage. A second capacitor Cc is also shown attached to the circuit. This capacitor is added across the base and collector of transistor Q6 and utilizes the Miller effect. Note that you should not add both capacitors C and Cc to the circuit at the same time. In last week's experiment you added a 680pF (or in some cases an 820pF) capacitor at the output of the second gain stage to stabilize the frequency response. This week we ask you to utilize capacitor Cc in a Miller configuration to stabilize the op-amp. Perform the following measurements on the complete op-amp circuit:

a- Note that the compensation capacitor C=680pF used for the op-amp is a fairly large capacitor. If we use the Miller capacitor Cc we will be able to reduce the amount of capacitance needed for compensation. Estimate the value of the Miller capacitor Cc required to produce the same bandwidth as measured last week with capacitor C used in the circuit. That is calculate the Miller capacitance Cc needed in place of capacitor C-680pF.

b- Measure the DC transfer characteristics of the complete amplifier, Vout vs. Vin. This measurement should be done similar to that in last week's experiment by ensuring that the amplifier offset voltage is eliminated (refer to Part II handout).

c- After measuring the transfer characteristics determine the offset voltage of the amplifier, and estimate its gain by calculating the slope of the Vout vs. Vin curve at the point where Vout =0V. Note that the slope of the dc transfer curve should be approximately equal to the ac gain that you will measure later.

d- Measure the differential and common-mode gains of the op-amp circuit, and its frequency response using the Miller capacitor Cc connected across the second gain stage of the op-amp. You will not need capacitor C=680pF at the output of the second gain stage if you use the Miller capacitor. Note that the gain values can be measured the same way as in last week's lab. Since the gain of the amplifier is very high you should try to

apply a DC offset at the input so that the output DC voltage with no ac input applied is equal to about zero (the output DC voltage should be measured by a voltmeter and not on the scope). Then you should apply your ac signal and measure the differential gain and the bandwidth. Make sure that you measure sufficient number of points so that you can plot the gain as a function of frequency and determine the upper cutoff frequency of the amplifier. You should then draw the Bode plot for the complete amplifier.

e- For the following measurements just use the 680pF capacitor (do not use the Miller capacitor). Verify the operation of your op-amp by constructing and measuring the low frequency gain, and the bandwidth of a non-inverting amplifier with a gain of approximately 100. (DO NOT USE RESISTORS LARGER THAN 2K FOR Rf, where Rf is the feedback resistor used in a standard non-inverting amplifier circuit).

f- Measure both the positive and negative slew-rate of your op-amp. (Measure slew-rate at Vout= 0 volts). You will see that the slew response of the op-amp will have a slightly different shape than what you may expect. We will discuss the reasons for some of these differences in class as we further discuss op-amp circuits.

LAB REPORT:

In your lab report you should summarize all of your measurement results obtained for the various circuits in Parts I, II, and III of this experiment. We expect you to include all of these measurements in a neat and clear fashion, making sure that you show all the circuits, the plots (like Bode and DC transfer curve) you obtained, and any important parameters (such as gain and offset) that you obtained from these plots. Make sure that you label all your figures, plots, tables, and clearly show your measured values so that your TA can easily find these measurements. If the report is not professionally done and if the measurement results are not clear you will loose points.

You should also present your hand calculations. You need not perform SPICE simulation for these circuits. Show hand calculated and measured results for the differential-mode and common-mode gains of the differential amplifier with resistive biasing, the output current and output resistance of the current mirror circuits, the differential-mode and common-mode gains of the differential pair with current-mirror biasing, the differential-mode and common-mode gains of the op-amp with the second gain stage added, the differential-mode and

common-mode gains of the complete op-amp circuit with the output stage added, and the gain and bandwidth of the non-inverting amplifier circuit constructed using your op-amp circuit. You should also compare the compensation of the op-amp using the 680pF capacitor and using the Miller compensation capacitor Cc.

Note that the format of this report is decided by you, and you can present any necessary discussions and findings that you feel are important. We would like to see a discussion of your overall findings in this lab, and your impression on how helpful this lab has been, and how it can be improved even further. Make sure that you present and discuss a summary of all the measurements that has been asked in the handouts for all parts of this experiment, and answer all the questions asked.

Data Sheet | February 7, 2006 | FN481.6

General Purpose High Current NPN Transistor Array

The CA3083 is a versatile array of five high current (to 100mA) NPN transistors on a common monolithic substrate. In addition, two of these transistors (Q_1 and Q_2) are matched at low current (i.e., 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
CA3083	CA3083	-55 to 125	16 Ld PDIP	E16.3
CA3083Z (Note)	CA3083Z	-55 to 125	16 Ld PDIP* (Pb-free)	E16.3
CA3083M96	3083	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3083MZ (Note)	3083MZ	-55 to 125	16 Ld SOIC (Pb-Free)	M16.15
CA3083MZ96 (Note)	3083MZ	-55 to 125	16 Ld SOIC (Pb-Free) Tape and Reel	M16.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

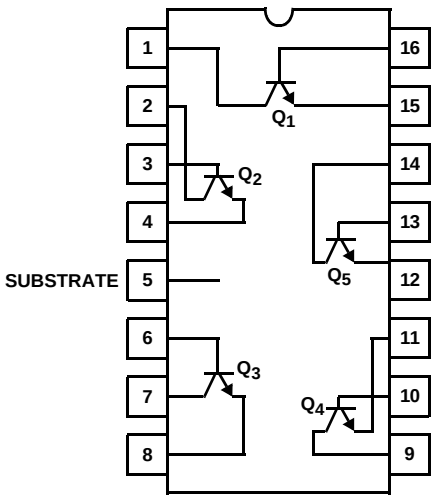
- High I_C . . . . . 100mA (Max)
- Low $V_{CE\ sat}$ (at 50mA). . . . . 0.7V (Max)
- Matched Pair (Q_1 and Q_2)
  - V_{IO} (V_{BE} Match). . . . . ±5mV (Max)
  - I_{IO} (at 1mA) . . . . . 2.5µA (Max)
- 5 Independent Transistors Plus Separate Substrate Connection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Signal Processing and Switching Systems Operating from DC to VHF
- Lamp and Relay Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing
- See Application Note AN5296 “Applications of the CA3018 Circuit Transistor Array” for Suggested Applications

Pinout

CA3083
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{ClO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current (I_C) 100mA
Base Current (I_B) 20mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	135	N/A
SOIC Package	200	N/A

Maximum Power Dissipation (Any One Transistor) 500mW
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate Terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

For Equipment Design, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
FOR EACH TRANSISTOR							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)ClO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0		5	6.9	-	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0		-	-	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0		-	-	1	μA
DC Forward-Current Transfer Ratio (Note 3) (Figure 1)	h_{FE}	V_{CE} = 3V	I_C = 10mA	40	76	-	
			I_C = 50mA	40	75	-	
Base-to-Emitter Voltage (Figure 2)	V_{BE}	V_{CE} = 3V, I_C = 10mA		0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage (Figures 3, 4)	$V_{CE\ SAT}$	I_C = 50mA, I_B = 5mA		-	0.40	0.70	V
Gain Bandwidth Product	f_T	V_{CE} = 3V, I_C = 10mA		-	450	-	MHz
FOR TRANSISTORS Q_1 AND Q_2 (As a Differential Amplifier)							
Absolute Input Offset Voltage (Figure 6)	$\|V_{IO}\|$	V_{CE} = 3V, I_C = 1mA		-	1.2	5	mV
Absolute Input Offset Current (Figure 7)	$\|I_{IO}\|$	V_{CE} = 3V, I_C = 1mA		-	0.7	2.5	μA

NOTE:

3. Actual forcing current is via the emitter for this test.

Typical Performance Curves

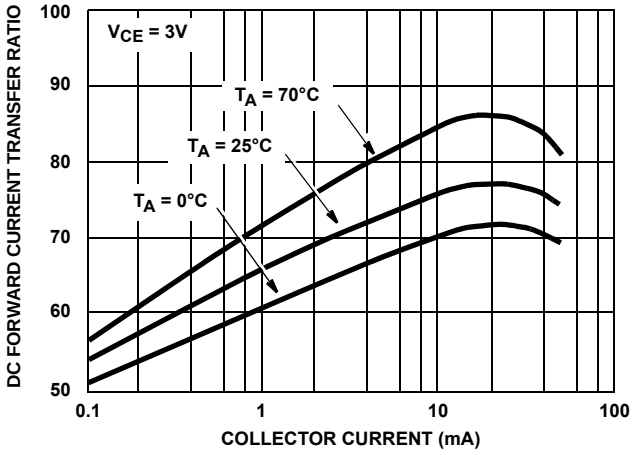


FIGURE 1. h_{FE} vs I_C

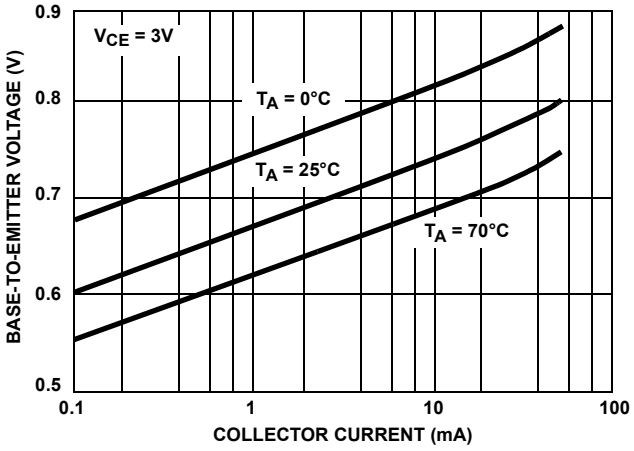


FIGURE 2. V_{BE} vs I_C

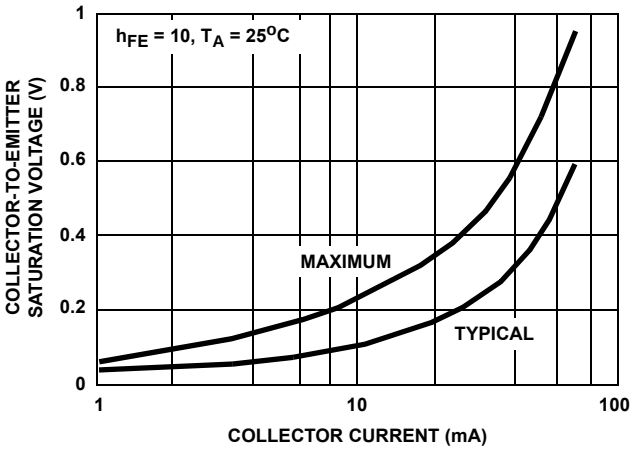


FIGURE 3. $V_{CE\ SAT}$ vs I_C

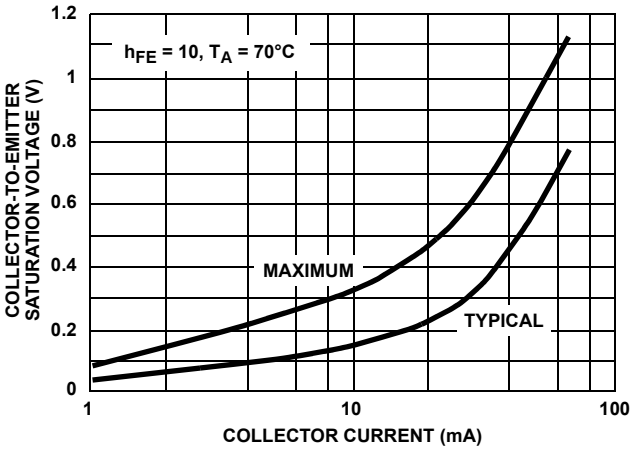


FIGURE 4. $V_{CE\ SAT}$ vs I_C

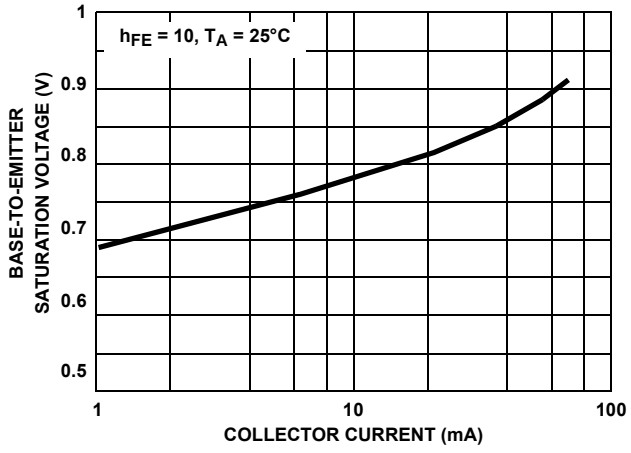


FIGURE 5. $V_{BE\ SAT}$ vs I_C

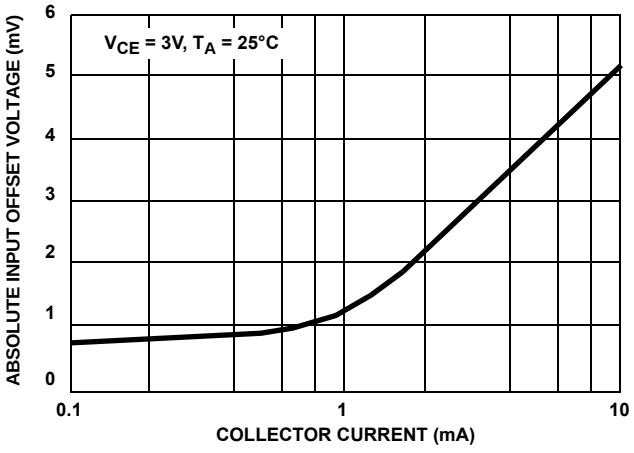


FIGURE 6. V_{IO} vs I_C (TRANSISTORS Q_1 AND Q_2 AS A DIFFERENTIAL AMPLIFIER)

Typical Performance Curves (Continued)

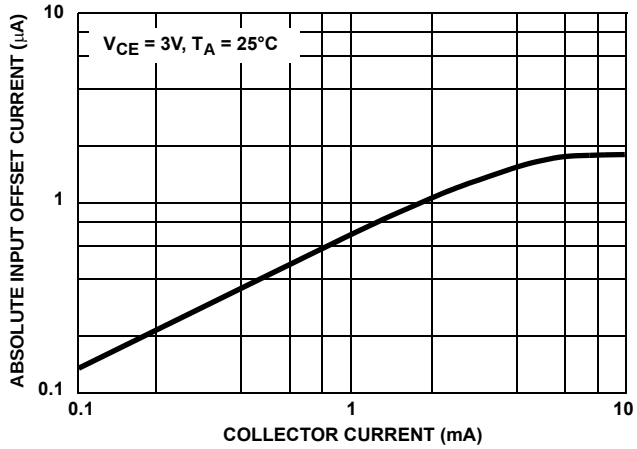
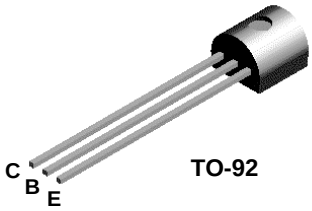


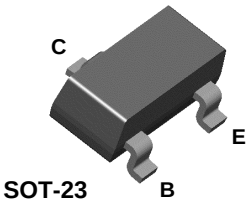
FIGURE 7. I_{IO} vs I_C (TRANSISTORS Q_1 AND Q_2 AS A DIFFERENTIAL AMPLIFIER)

FAIRCHILD
SEMICONDUCTOR TM

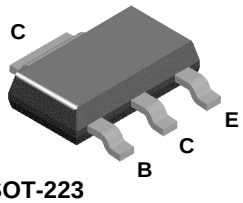
2N3904 MMBT3904 PZT3904



TO-92



SOT-23
Mark: 1A



SOT-223

NPN General Purpose Amplifier

This device is designed as a general purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3904	*MMBT3904	**PZT3904	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

NPN General Purpose Amplifier
(continued)

Electrical Characteristics
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	6.0		V
I_{BL}	Base Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V I_C = 1.0 mA, V_{CE} = 1.0 V I_C = 10 mA, V_{CE} = 1.0 V I_C = 50 mA, V_{CE} = 1.0 V I_C = 100 mA, V_{CE} = 1.0 V	40 70 100 60 30	 300 	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA		0.2 0.3	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA	0.65	0.85 0.95	V V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz		4.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 1.0 MHz		8.0	pF
NF	Noise Figure	I_C = 100 μA, V_{CE} = 5.0 V, R_S =1.0kΩ,f=10 Hz to 15.7kHz		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V, I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_r	Rise Time			35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10mA I_{B1} = I_{B2} = 1.0 mA		200	ns
t_f	Fall Time			50	ns

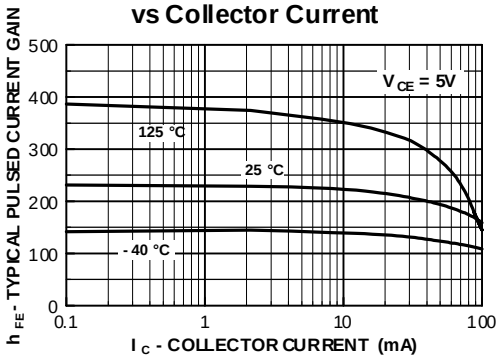
*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Spice Model

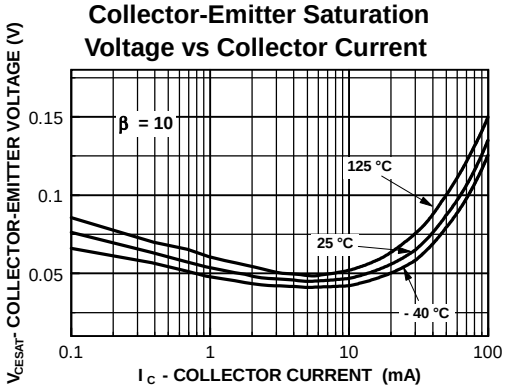
NPN (Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259 Ise=6.734 Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75 Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)

Typical Characteristics

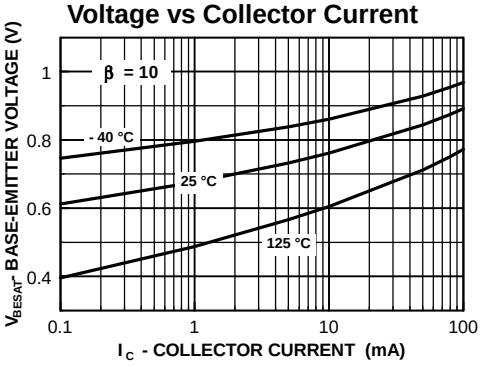
Typical Pulsed Current Gain vs Collector Current



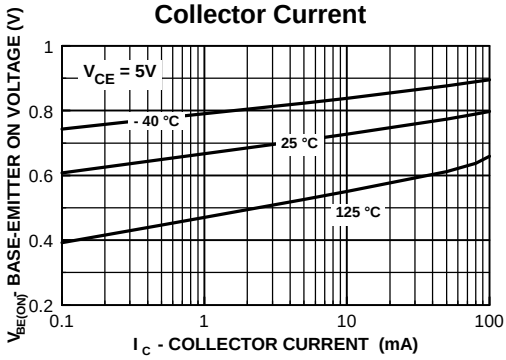
Collector-Emitter Saturation Voltage vs Collector Current



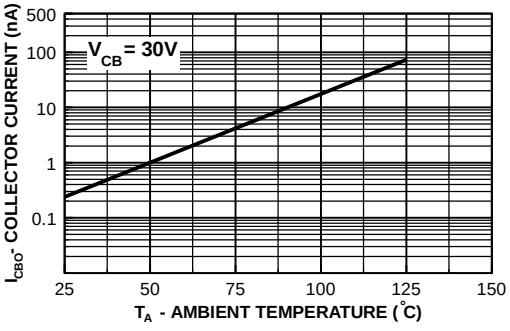
Base-Emitter Saturation Voltage vs Collector Current



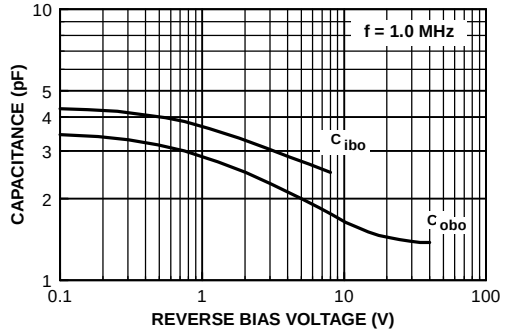
Base-Emitter ON Voltage vs Collector Current



Collector-Cutoff Current vs Ambient Temperature

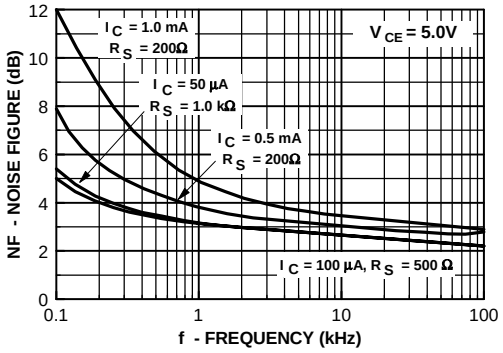


Capacitance vs Reverse Bias Voltage

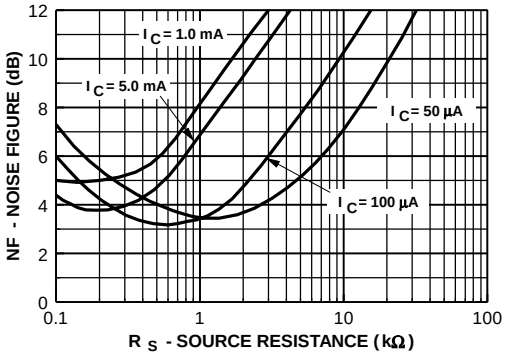


Typical Characteristics (continued)

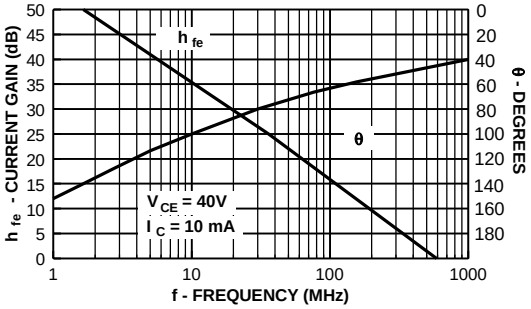
Noise Figure vs Frequency



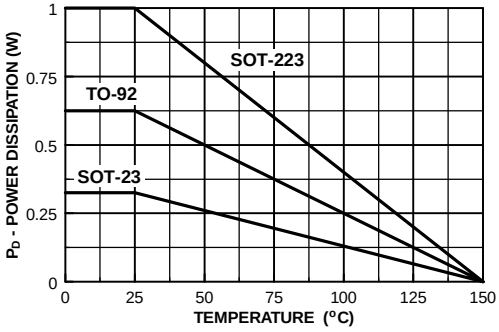
Noise Figure vs Source Resistance



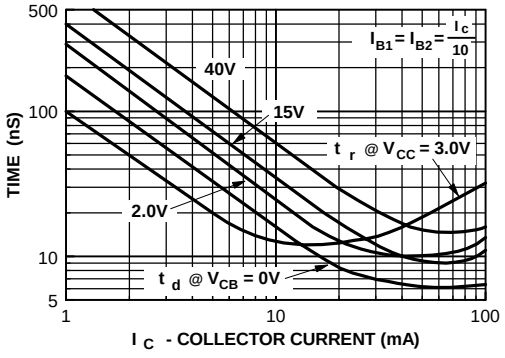
Current Gain and Phase Angle vs Frequency



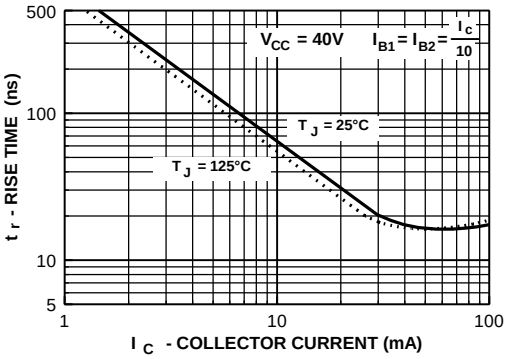
Power Dissipation vs Ambient Temperature



Turn-On Time vs Collector Current

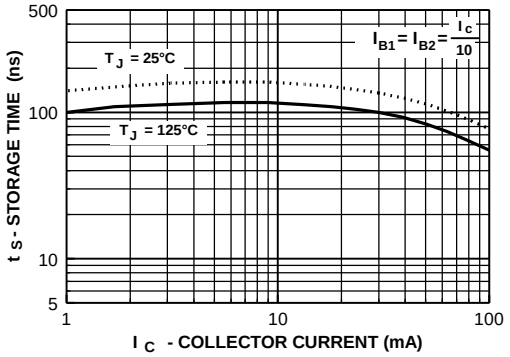


Rise Time vs Collector Current

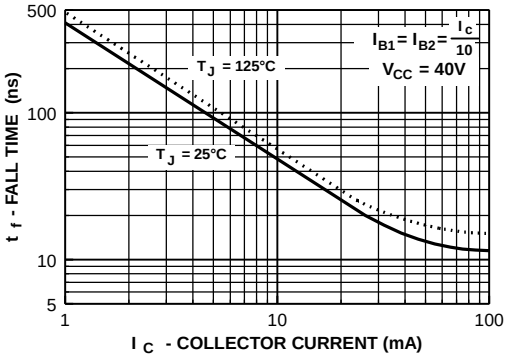


Typical Characteristics (continued)

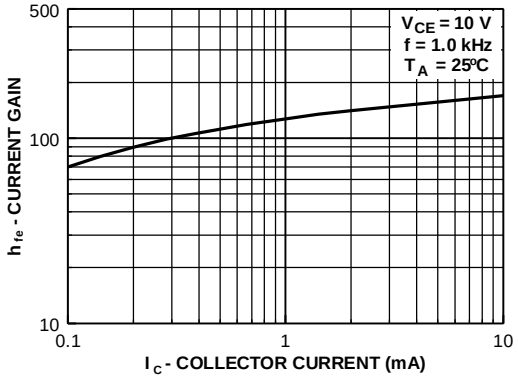
Storage Time vs Collector Current



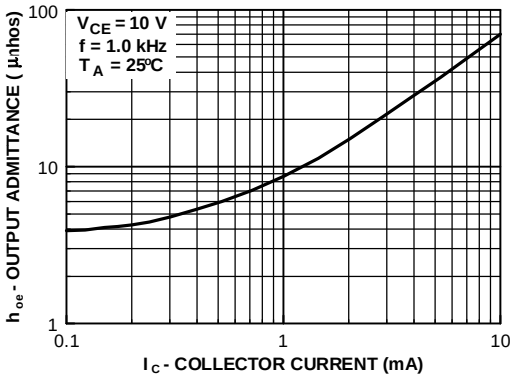
Fall Time vs Collector Current



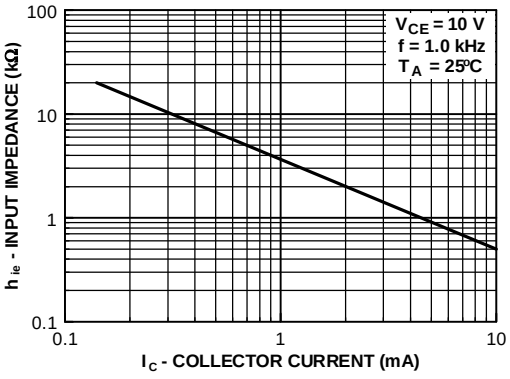
Current Gain



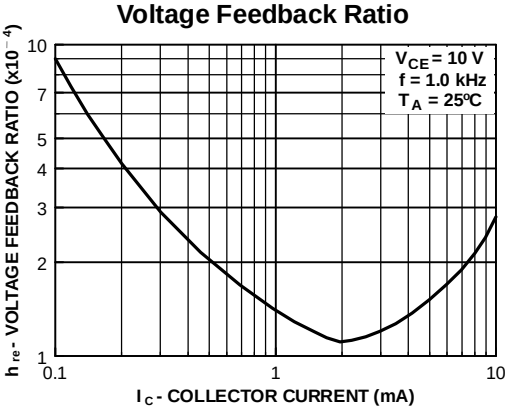
Output Admittance



Input Impedance



Voltage Feedback Ratio



Test Circuits

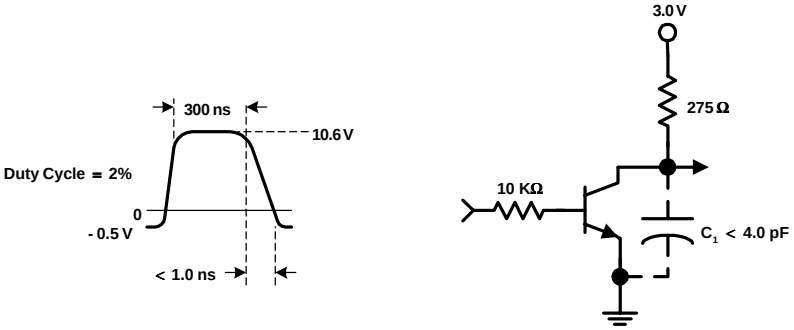


FIGURE 1: Delay and Rise Time Equivalent Test Circuit

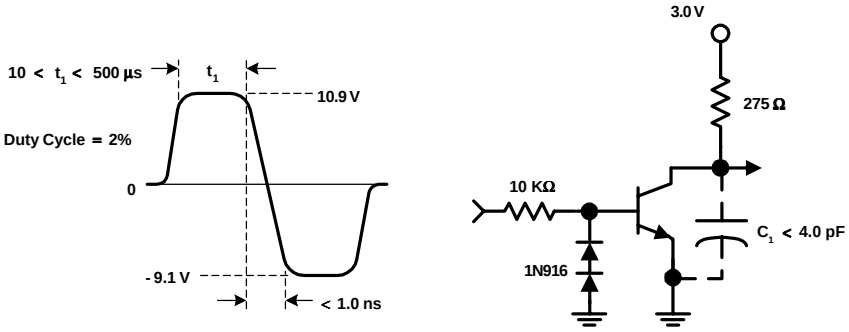
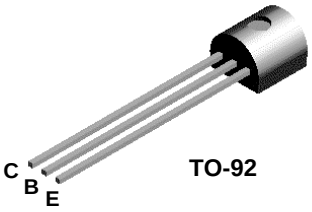


FIGURE 2: Storage and Fall Time Equivalent Test Circuit

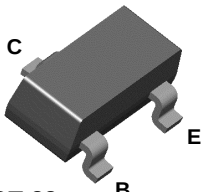
FAIRCHILD SEMICONDUCTOR™

Jameco Part Number 38375

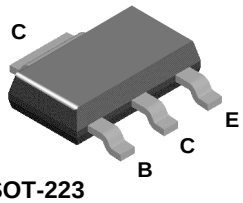
2N3906 MMBT3906 PZT3906



TO-92



SOT-23
Mark: 2A



SOT-223

PNP General Purpose Amplifier

This device is designed for general purpose amplifier and switching applications at collector currents of 10 μA to 100 mA.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	40	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
3) All voltages (V) and currents (A) are negative polarity for PNP transistors.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3906	*MMBT3906	**PZT3906	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

PNP General Purpose Amplifier
(continued)

Electrical Characteristics
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage*	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 µA, I_E = 0	40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 µA, I_C = 0	5.0		V
I_{BL}	Base Cutoff Current	V_{CE} = 30 V, V_{BE} = 3.0 V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{BE} = 3.0 V		50	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain *	I_C = 0.1 mA, V_{CE} = 1.0 V I_C = 1.0 mA, V_{CE} = 1.0 V I_C = 10 mA, V_{CE} = 1.0 V I_C = 50 mA, V_{CE} = 1.0 V I_C = 100 mA, V_{CE} = 1.0 V	60 80 100 60 30	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA		0.25 0.4	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA	0.65	0.85 0.95	V V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	250		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 100 kHz		4.5	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 100 kHz		10.0	pF
NF	Noise Figure	I_C = 100 µA, V_{CE} = 5.0 V, R_S =1.0kΩ,f=10 Hz to 15.7 kHz		4.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V, I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_r	Rise Time			35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10mA I_{B1} = I_{B2} = 1.0 mA		225	ns
t_f	Fall Time			75	ns

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

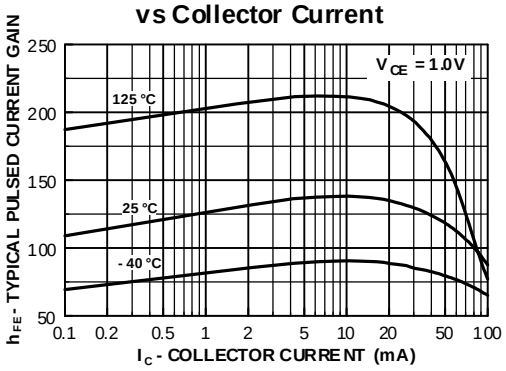
NOTE: All voltages (V) and currents (A) are negative polarity for PNP transistors.

Spice Model

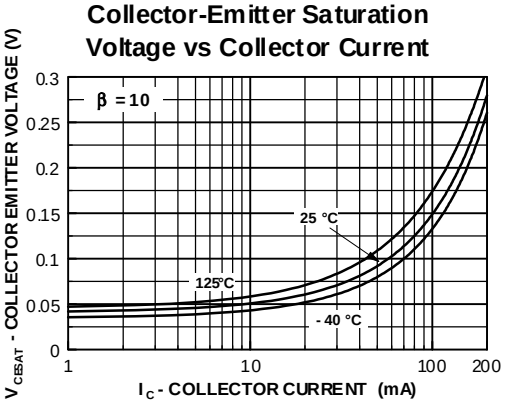
PNP (Is=1.41f Xti=3 Eg=1.11 Vaf=18.7 Bf=180.7 Ne=1.5 Ise=0 Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p Mjc=.5776 Vjc=.75 Fc=.5 Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)

Typical Characteristics

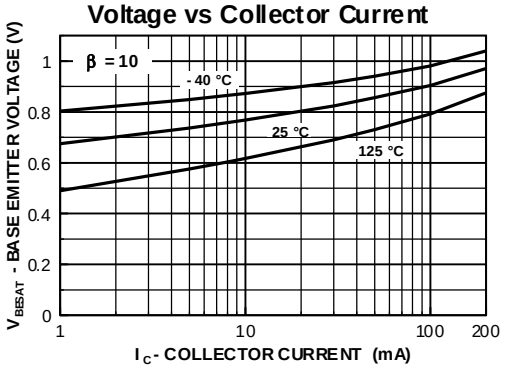
Typical Pulsed Current Gain vs Collector Current



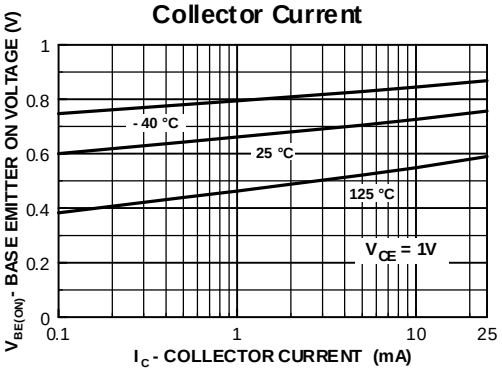
Collector-Emitter Saturation Voltage vs Collector Current



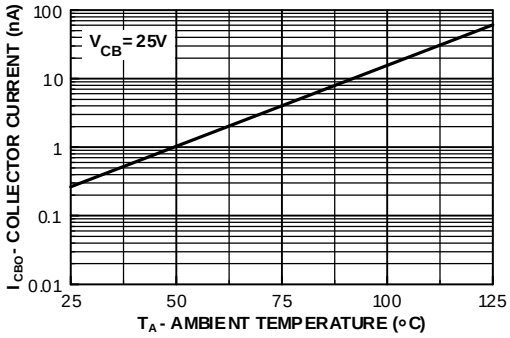
Base-Emitter Saturation Voltage vs Collector Current



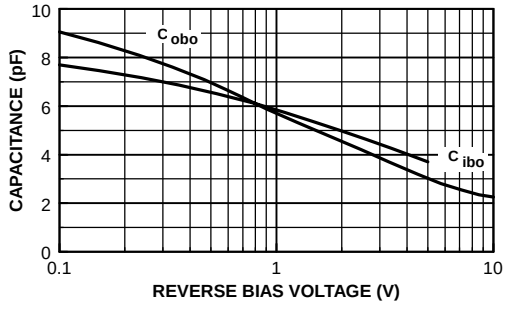
Base Emitter ON Voltage vs Collector Current



Collector-Cutoff Current vs Ambient Temperature

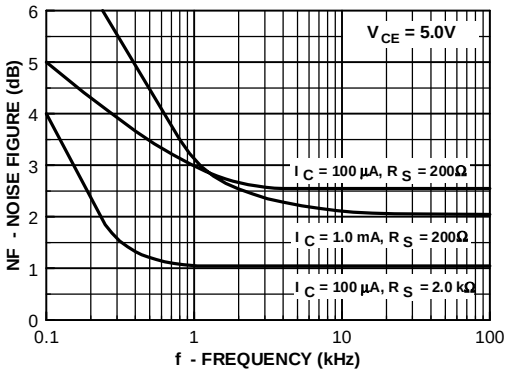


Common-Base Open Circuit Input and Output Capacitance vs Reverse Bias Voltage

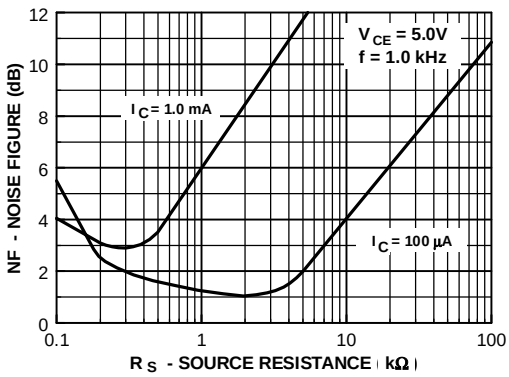


Typical Characteristics (continued)

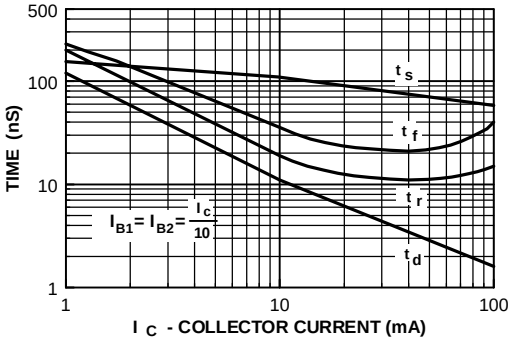
Noise Figure vs Frequency



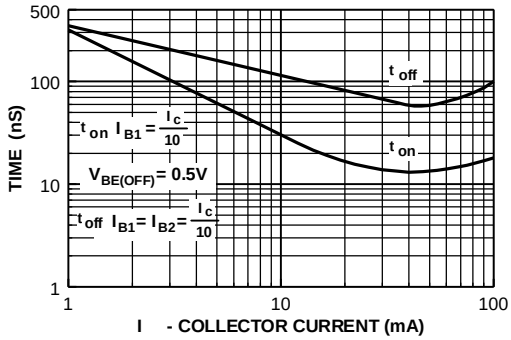
Noise Figure vs Source Resistance



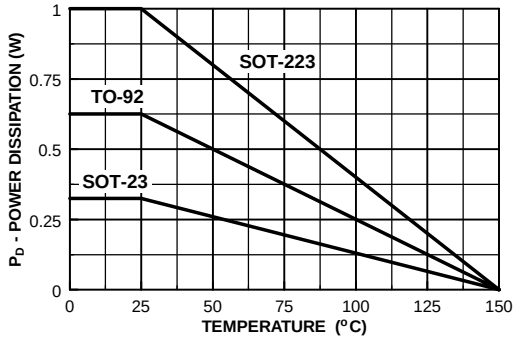
Switching Times vs Collector Current



Turn On and Turn Off Times vs Collector Current

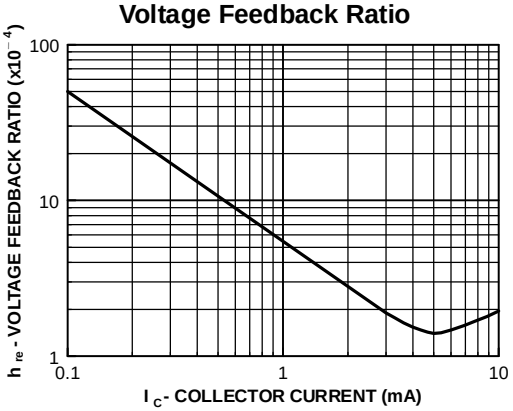


Power Dissipation vs Ambient Temperature

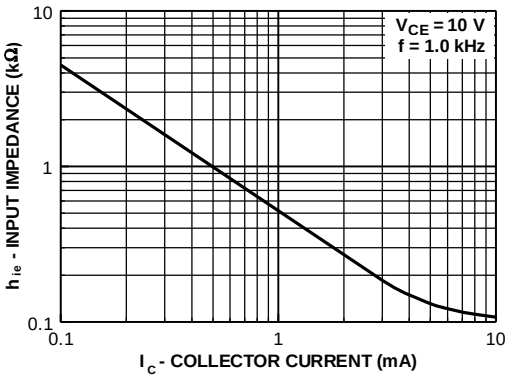


Typical Characteristics (continued)

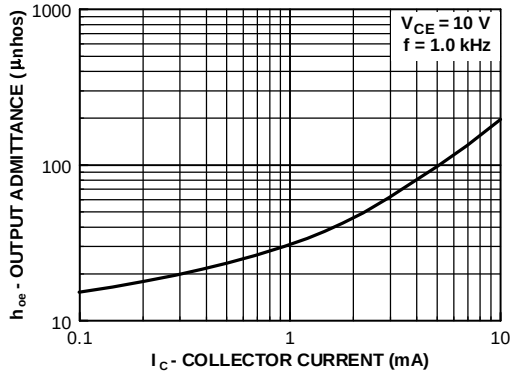
Voltage Feedback Ratio



Input Impedance



Output Admittance



Current Gain