

Lecture 18: Output Stages

Announcements:

- ↳ Graded Midterm Exam: will hand back with solutions towards the end of lecture today
- ↳ HW#8 online
- ↳ Lab#3 online today
- ↳ I will be traveling on Thursday, so need to do a make-up lecture
- ↳ Make-Up Lecture: Wednesday, 3/30, 7-8:30 p.m., in 521 Cory (the Hogan room)
- ↳ Again, I will be using software local to my computer to record the lecture

Lecture Topics:

- ↳ Go through Lab#3
- ↳ Output Stages
- ↳ Class A & B
- ↳ Go through Midterm Exam & hand back

Last Time:

Output Stages

- Class A (Emitter or Source Follower)
- Class B
- Class AB (we'll do this one later)

Purpose: Drive Loads

- ① Deliver power w/ small distortion.
- ② Minimize output impedance → so that the amplifier gain is insensitive to the load.

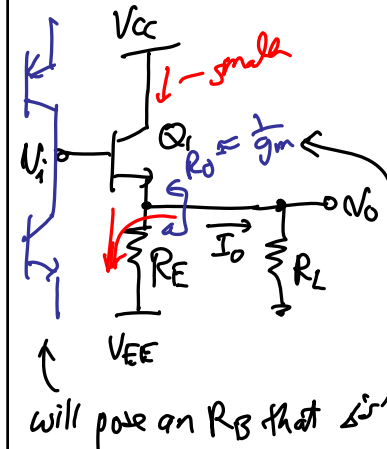


$$\frac{N_o}{N_i} = \frac{R_i}{R_L + R_o}$$

Desirable Attributes:

- ① High R_{in} ; Low R_{out} .
- ② Low quiescent power.
- ③ Minimal effect on the amplifier freq. response. *very high freq. poles*
- ④ Should be able to handle large input/output swings. (i.e., V_i may be $> V_T$, invalidating small-signal approximations)

Emitter Follower (Class A)



Two Main Cases:

- ① $I_o > 0$: I_o comes from Q_1 , → adequate I_o can be supplied so long as Q_1 stays in forward-active

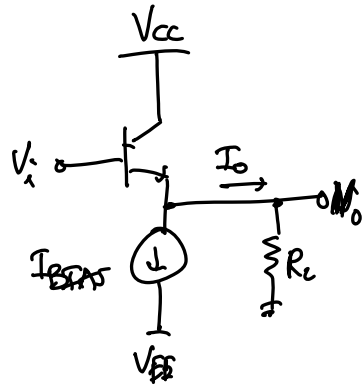
- ② $I_o < 0$: (i.e., $V_o < 0$) I_o must be sunk to V_{EE} through R_E

$$I_o = \frac{V_o - V_{EE}}{R_E} \rightarrow \text{gets smaller as } V_o \downarrow \text{ as } V_o \downarrow \rightarrow I_o \downarrow$$

Problem!

↓ solution

Solution: Replace RE w/ a current source

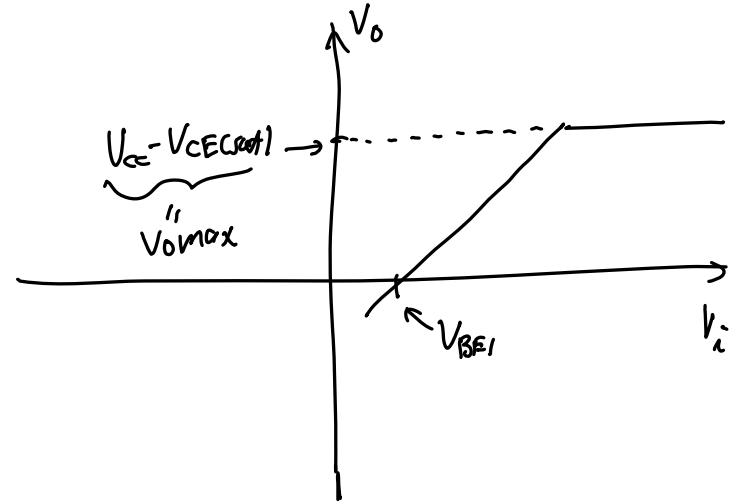
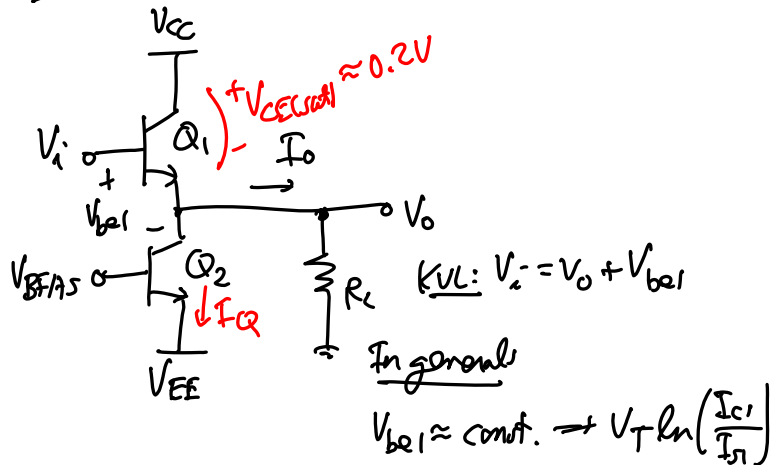


Now, can source I_o thru R_L for C_{th} gets V_o .

And can sink $I_o = I_{EAS}$ (a lot)

$\frac{1}{2} I_o$ does not get smaller as V_o decreases
can maintain drive power!

Actual Implementation



Two Cases:

Case ①: R_L large $\rightarrow I_o < I_Q$

$\Rightarrow I_o$ not doing much to get a large ΔV_o

For V_i large and (1): Q_1 must source $I_o + I_Q$ to make $V_o \uparrow$

at same pt., Q_2 will saturate as $V_o \uparrow$

$$V_{max} = V_{cc} - V_{CE(sat)}$$

$$\text{and } V_i = V_{cc} - V_{CE(sat)} + V_{BE1}$$

not always possible if input signal is limited by V_{cc} supply rail

- Now, distribute graded midterm exams and go through grading and what everything means