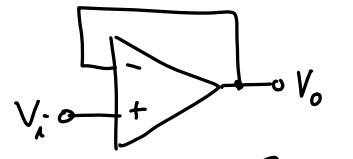
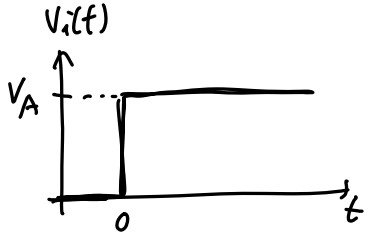
Lecture 24: Slew Rate, Settling Time, & PSRR

- Announcements:
- Design Project Checkpoint:
  - Due Monday, April 25, 11:59 p.m.
  - Send to your TA a spice file for your op amp design that simulates correctly, i.e., that reaches a stable bias point where all transistors are saturated (or linear if an MOS resistor)
  - It doesn't need to meet the project specs, but it should simulate correctly
- Lecture Topics:
  - Slew Rate (revisited)
  - Settling Time
  - Power Supply Rejection Ratio (PSRR)
- ----------
- Last Time: finished compensation

Slew Rate (from before)





Using Laplace Xform Theory:

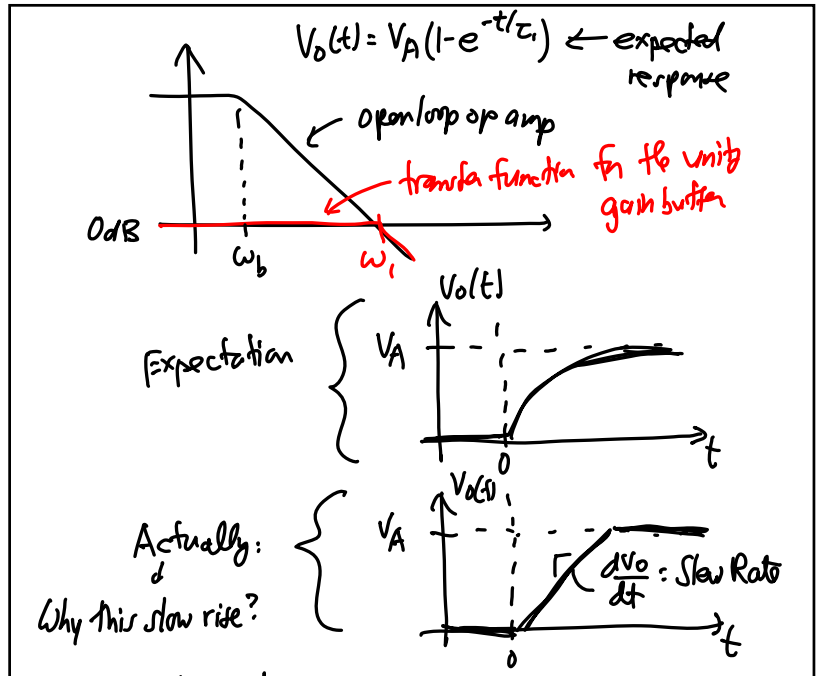
$$\frac{V_o}{V_i}(s) = \frac{1}{1+\frac{s}{\omega_1}} = \frac{1}{1+s\tau_1}$$

← single (dominant) pole

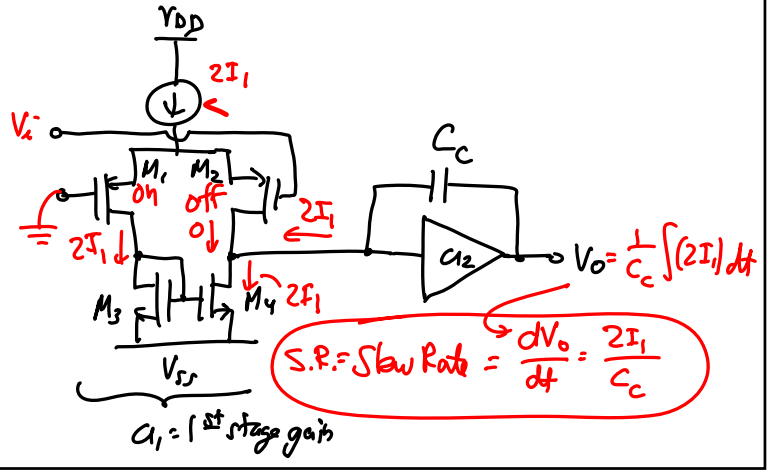
$$V_i(s) = \frac{V_A}{s}$$

$$V_o(s) = \frac{V_A}{s(1+s\tau_1)} = \frac{V_A}{s} - \frac{V_A}{s+\frac{1}{\tau_1}}$$

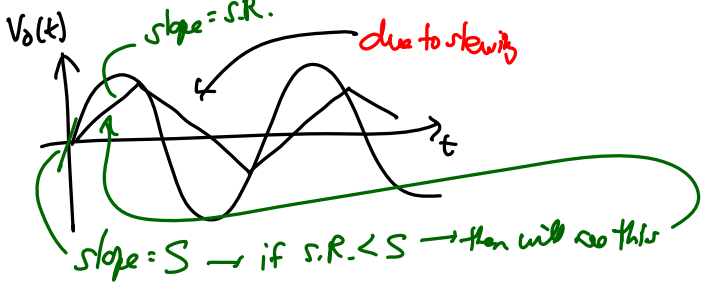
⇕ Inverse Laplace Xform



Reason: 1st or 2nd stage of op amp cannot source enough current to mimic the slope (or speed) of a fast rising input signal.



If apply a very fast (i.e., high freq., large amplitude) sinusoid:



S.R. in terms of Design Variables

$$S.R. = \frac{dV_o}{dt} = \frac{2I_1}{C_c} = \frac{2I_1}{G_{m1}}\omega_{ugf}A_o = S.R.$$

($2I_1$ = tail current)

$$\left[C_c = \frac{G_{m1}}{\omega_{ugf}A_o}\right]$$

A_o ↑ closed loop gain

ω_{ugf} ↑ ω @ $|T(j\omega)| = 1$

To Increase S.R.:

① Decrease G_{m1} ← transconductance of 1st stage

② Increase ω_{ugf} → increase ω_2
↘ limited by the technology freq. range

③ Use a larger A_o, if possible.
↑ closed loop gain
↓ (only if permitted by the application)

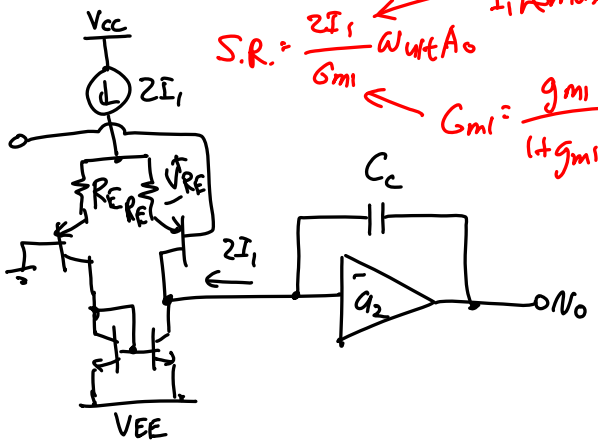
Increasing S.R. via G_m-Reduction

① Emitter or Source Degeneration of the Input Stage—

I_1 remains same

$$S.R. = \frac{2I_1}{G_{m1}}\omega_{ugf}A_o$$

$$G_{m1} = \frac{g_{m1}}{1+g_{m1}R_E} \downarrow \Rightarrow SR\uparrow$$



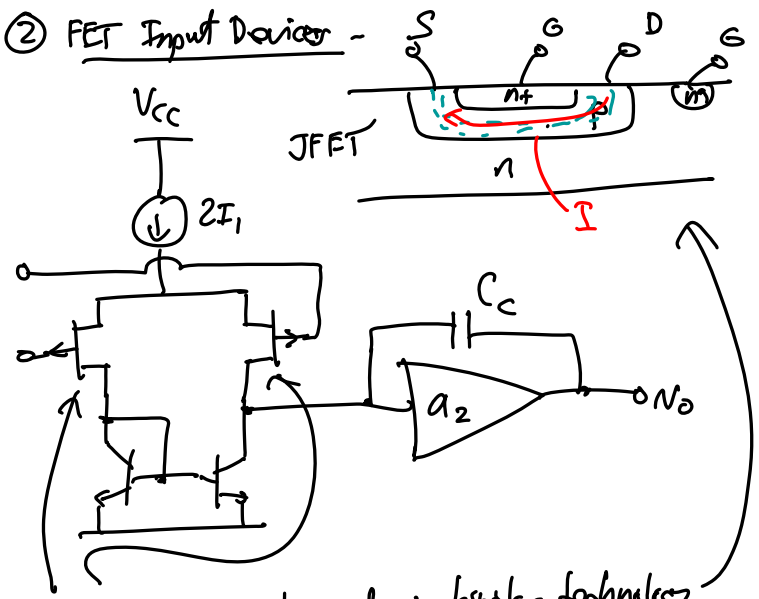
Limitations:

① R_E mismatch → V_{os}
↳ must limit V_{RE} to limit V_{os}

② R_E↑ → gain↓ (SR-gain trade-off)

③ R_E contributes thermal noise → must limit to preserve the noise performance of the op amp.

② FET Input Devices -



JFET's → can be made in bipolar technology → very large R_i

For FET's: $\frac{g_m}{I_D} \simeq \frac{2}{V_{GS}-V_t}$ } ~0.2V

For BJT's: $\frac{g_m}{I_C} = \frac{1}{V_T}$ } ~26mV

$$\frac{\text{FET S.R.}}{\text{BJT S.R.}} = \frac{\frac{I_D}{g_{mF}}\omega_{ulf}}{\frac{I_C}{g_{mB}}\omega_{ulf}} = \frac{\frac{V_{GS}-V_t}{2}}{V_T} \rightarrow \text{large \#}$$

Limitations.
① High V_{OS}.
② Increased voltage noise (but decreased current noise)

Settling Time

response to a step V_i:

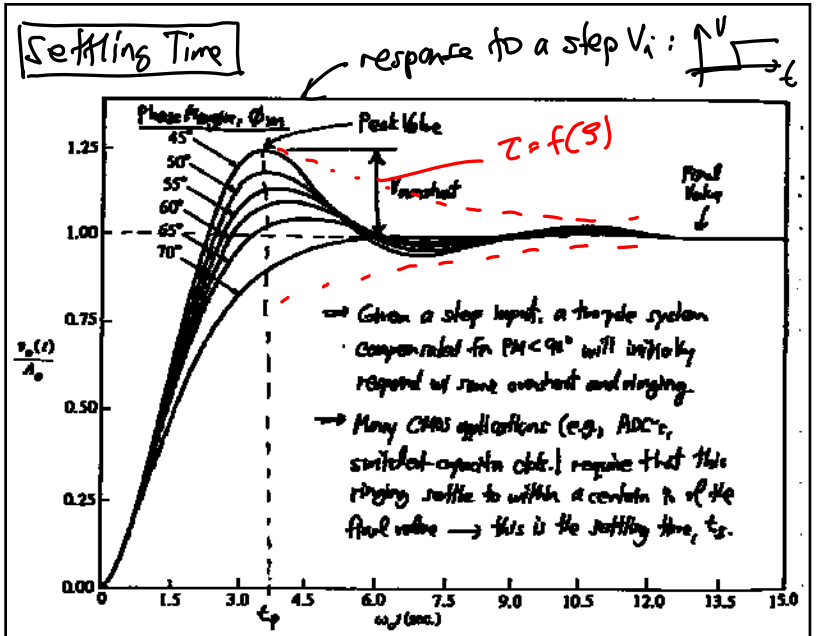


Figure 8.2-3 Response of second-order system with various phase margins.

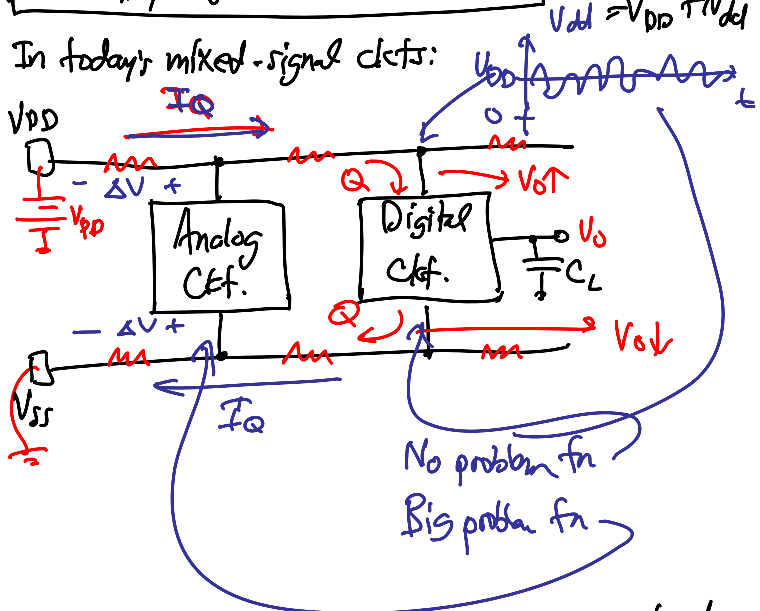
Obtain Expressions fn:

① $V_{overshoot}$
② Settling Time, T_s
} as functions of phase margin, ϕ_m

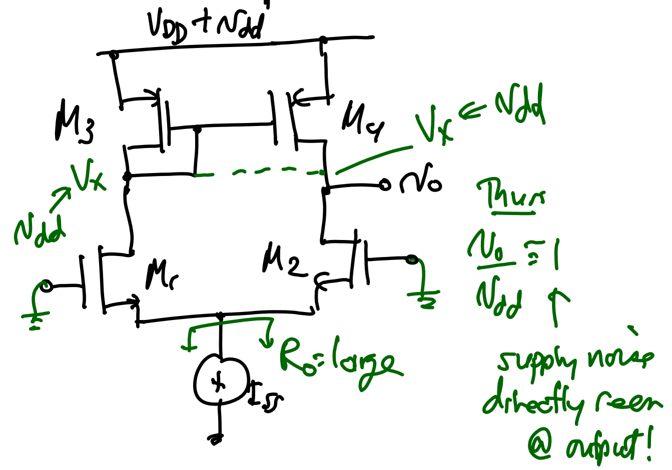
- Go through settling time handout

Power Supply Rejection Ratio (PSRR)

In today's mixed-signal ckts:



Ex. CMOS Diff. Input Stage w/ Current Source Load



Definition: Power Supply Rejection Ratio (PSRR)

$$PSRR \triangleq \frac{\text{Gain from Input to Output}}{\text{Gain from Supply to Output}} = \frac{A_v|_{v_{dd}=0}}{A_{dd}|_{v_i=0}}$$

Thus, for the above example: $PSRR \cong \frac{g_{m2}(r_{o2}||r_{o4})}{1}$

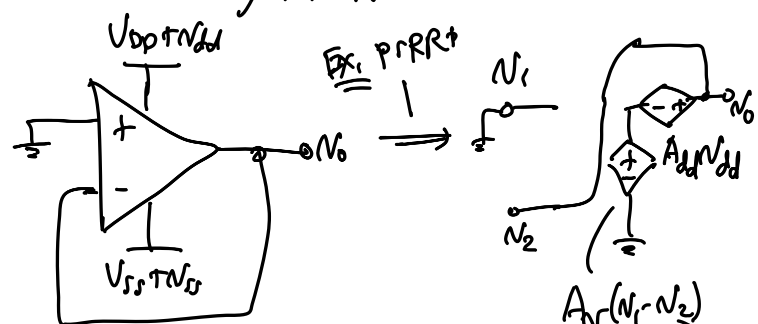
→ $PSRR \cong g_{m2}(r_{o2}||r_{o4})$

For more complicated ckts, much more is involved.

↳ to make it easier, use a unity gain config.

↳ can also get $PSRR = f(\omega)$

Ex. $PSRR^+$



$$v_o = A_v(v_1 - v_2) + A_{dd} v_{dd}, \quad v_1 - v_2 = -v_o$$

$$v_o(1 + A_v) = A_{dd} v_{dd}$$

$$\frac{v_o}{v_{dd}} = \frac{A_{dd}}{1 + A_v} = \frac{1}{\frac{1}{A_{dd}} + \frac{A_v}{A_{dd}}} \approx \boxed{\frac{1}{PSRR^+} = \frac{v_o}{v_{dd}}}$$

$A_v(v_1 - v_2)$

$$\boxed{PSRR^+ = \frac{v_{dd}}{v_o}}$$