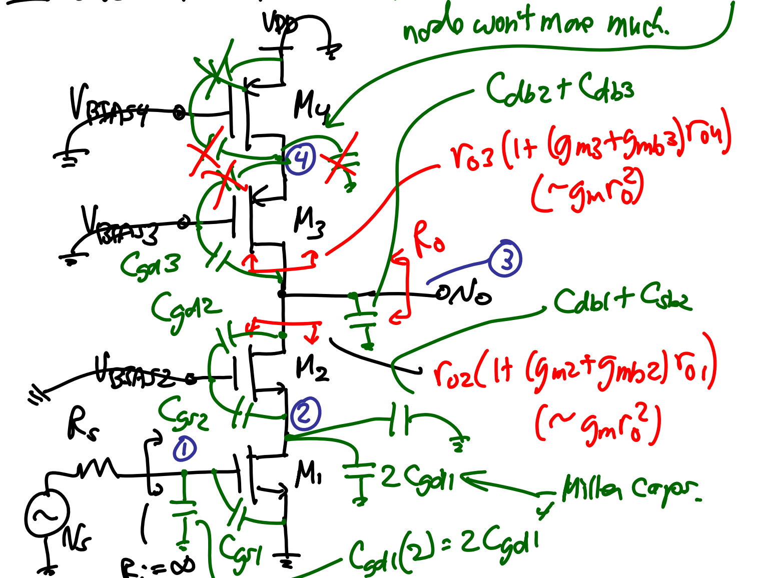
Lecture 9: Current Sources

- **Announcements**: → Labs on Monday → shift to next Monday
  - HW#4 passed out today (and online)
  - Lab#2 passed out today (and online)
  - Monday Labs: due to holiday next week, shift to the following Monday
  - Monday Lab#1's are due in the 140 Box on Tuesday next week (per Travis's email)
- **Lecture Topics**:
  - Current Sources
  - Current Source V_{BIAS} Generators
  - Output Swing (Headroom)
- -------------------------------------
- **Last Time**:

Ex. Cascode Drive & Load

For reasons to be discussed, this node won't move much.



$$R_o = r_{o2}(1+(g_{m2}+g_{mb2})r_{o1}) \,\|\, r_{o3}(1+(g_{m3}+g_{mb3})r_{o4})$$

$$A_v = \frac{v_{①}}{v_s}\cdot\frac{v_{②}}{v_{①}}\cdot\underbrace{\frac{v_o}{v_{②}}}_{\approx -1}$$

$$= (1)\left(-g_{m1}\left(\frac{1}{\cancel{g_{m2}+g_{mb2}}}\right)\right)(\cancel{g_{m2}+g_{mb2}})R_o$$

$$\therefore \boxed{A_v = -g_{m1}R_o}$$

Get the dominant pole: (use OCTC analysis)

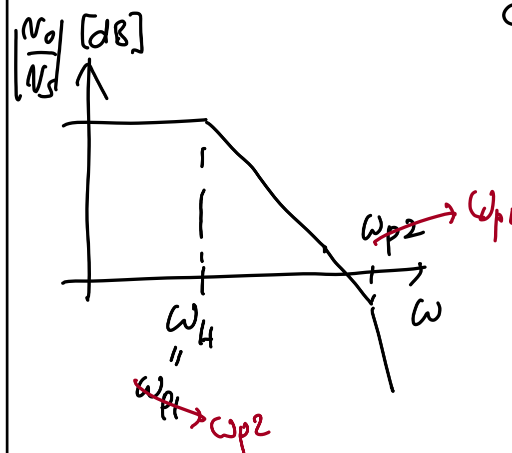
$\tau_{①} = (2C_{gd1} + C_{gs1})R_s$

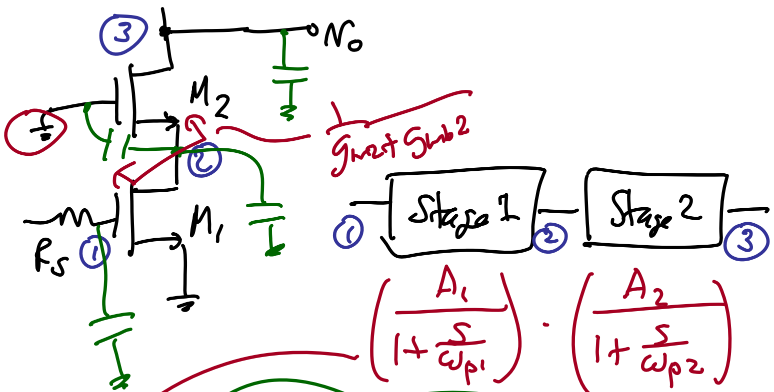
$\tau_{②} = (2C_{gd1} + C_{gs2} + C_{db1} + C_{sb2})\left(\frac{1}{g_{m2}+g_{mb2}}\right)$

$\tau_{③} = (C_{gd2} + C_{db2} + C_{db3} + C_{gd3})R_o$ ← huge

$$\omega_H = \frac{1}{\tau_{①} + \tau_{②} + \tau_{③}}$$

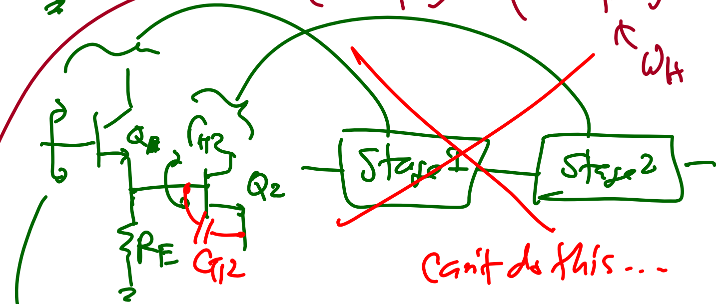
⇒ this is accurate enough... but... can we be a bit smarter?





$$\left(\frac{A_1}{1+\frac{s}{\omega_{p1}}}\right)\cdot\left(\frac{A_2}{1+\frac{s}{\omega_{p2}}}\right)$$

ω_H



$r_\pi + (\beta+1)(R_E \| r_{\pi 2} \| r_{o1})$

This impedance affected by next stage.

Can separate the T.F.'s:

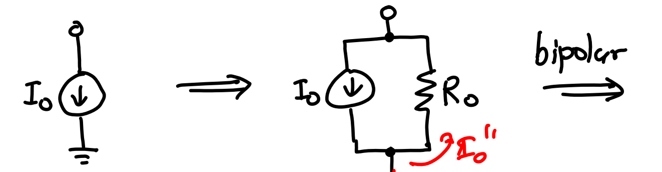
So:

(i) Node ③ contributes the dominant pole: $\boxed{\omega_{p2} = \frac{1}{\tau_3}}$

(ii) Capacitors associated w/ ① & ② contribute the 2nd pole: $\boxed{\omega_{p1} = \frac{1}{\tau_1 + \tau_2}}$

Transistor Current Sources

How can a transistor implement a current source?



Ideal Current Source

Actual Current Source

$R_o = \infty \rightarrow$ ideal

I_o' R_L

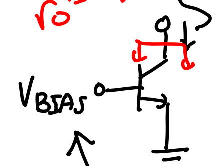
maxi'ed (good) when R_o = big

Bipolar

Forward-Active Xsistor Current Source

want accurate

r_o = huge $\quad I_o = I_C = I_S \exp\left(\frac{V_{BIAS}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$



Very stable if V_{BIAS} = const. & V_A = large

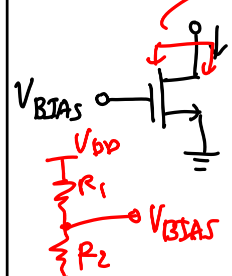
Note that V_{BIAS} must be very accurate due to exponential
→ to several sig. figs.
e.g., $V_{BIAS} = 0.68745V$

MOS

Saturated MOS Xsistor Current Source

$R_o = r_o$ = large

$I_o = I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{BIAS} - V_t)^2(1 + \lambda V_{DS})$



Again, very stable if V_{BIAS} = const. & λ = small

Problem: need to generate a stable V_{BIAS}

We now focus on methods for generating V_{BIAS}.

But how do we get this degree of precision using a transistor ckt?

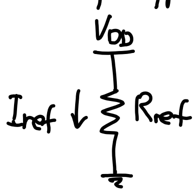
Solution:

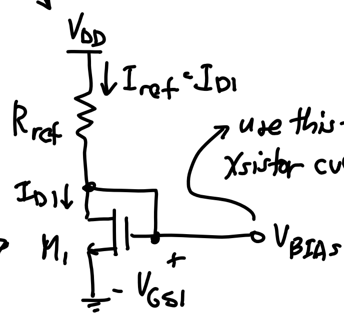
Replica Biasing (a simple & effective approach)

1. Generate the desired current.
2. Push the current through a Xsistor and allow it to reach a stable bias pt.
3. Use this stable bias pt. as V_{BIAS}

this can be very precise!

One simple approach:





use this to bias a Xsistor current source!

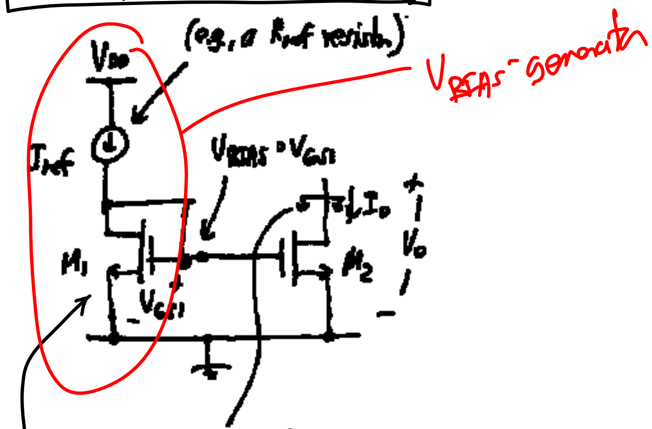
A diode connected Xsistor is always in saturation and will basically bias itself to support the needed current!

$$I_{ref} = I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1}-V_t)^2(1+\lambda V_{DS1})$$

V_{BIAS}

Now, can distribute this V_{BIAS} to the gates of many MOS transistor current sources!

Ex. Simple MOS Current Source



$R_o = r_o = \frac{1}{\lambda I_o}$

Diode-connected Xsistor → saturation:

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{BIAS}-V_t)^2(1+\lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{BIAS}-V_t)^2(1+\lambda V_{DS2})$$

In general, $V_{DS1} \neq V_{DS2}$, but if λ = small, then little difference in I_{D1} & I_{D2}

1. Case: matched M_1 & M_2 ⟹ $I_o = I_{ref}$
2. Case: M_1 & M_2 scaled w.r.t. to each other

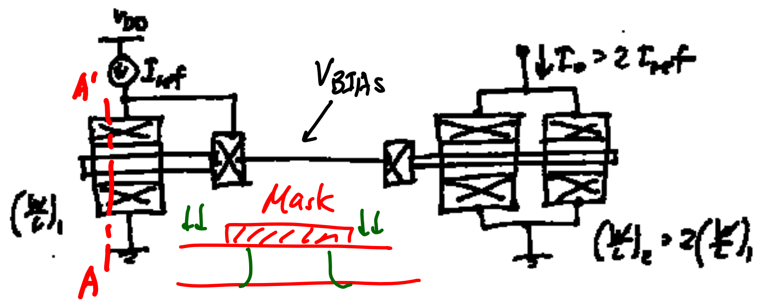
⟹ $\boxed{I_o = I_{ref}\frac{(W/L)_2}{(W/L)_1}}$

⟹ use $L_1 = L_2$ for better accuracy, then:

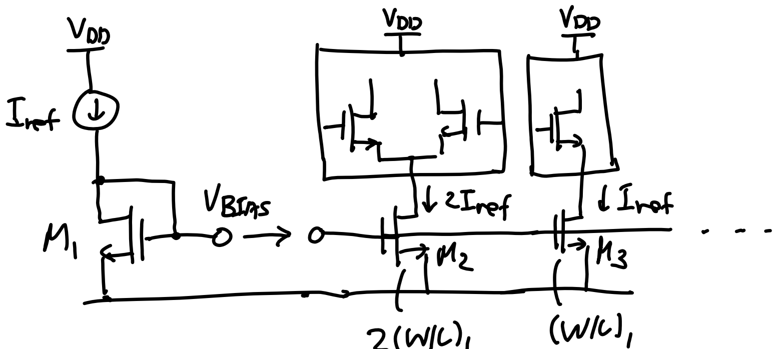
$$\boxed{\frac{I_o}{I_{ref}} = \frac{W_2}{W_1}}$$

Note: For better accuracy, should use multiple copies of one device when scaling current → reduces edge effects!

Ex: Layout for a Doubling Current Source

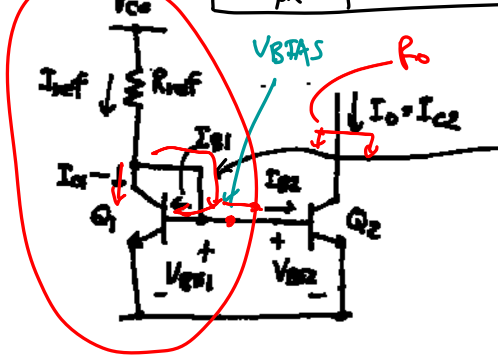


A single V_{BIAS} generator can now serve numerous current sources:



How about bipolar? V_{BIAS} Generator

Simple Bipolar Current Source



KCL here to get $I_{C2} = f(I_{ref})$

Assume Q_1 & Q_2 are matched.

i.e., $V_A = \infty$

$V_{BE1} = V_{BE2} \longrightarrow I_{C1} = I_{C2} = I_o$ (neglecting V_A's)

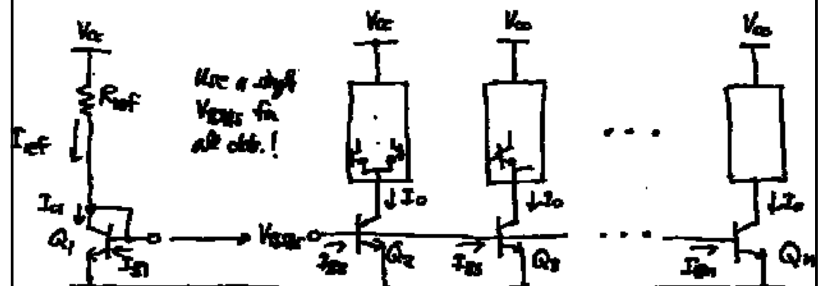
KCL: $I_{ref} = I_{C1} + I_{B1} + I_{B2} = I_{C1}\left(1 + \frac{2}{\beta}\right)$

$\therefore I_{C1} = I_{C2} = \boxed{I_o = \frac{I_{ref}}{1 + \frac{2}{\beta}}} \longrightarrow I_o \approx I_{ref}$

can say error $\sim \frac{2}{\beta}$

and $\boxed{I_{ref} = \frac{V_{CC} - V_{BE(on)}}{R_{ref}}}$ $0.7V$ $\boxed{R_o = r_{o2}}$

Again, a single V_{BIAS} generator can serve many current sources throughout the IC chip:



$I_{ref} = I_{C1} + I_{B1} + I_{B2} + I_{B3} + \cdots + I_{Bn}$

[Identical Xistors] $\Longrightarrow I_{ref} = I_{C1}\left(1 + \frac{n}{\beta}\right)$

$\Longrightarrow \boxed{I_o = I_{C1} = \frac{I_{ref}}{\left(1 + \frac{n}{\beta}\right)}}$

Problem: error $\sim \frac{n}{\beta}$ increases as n (I_o deviates from I_{ref}, and the deviation depends on n.)

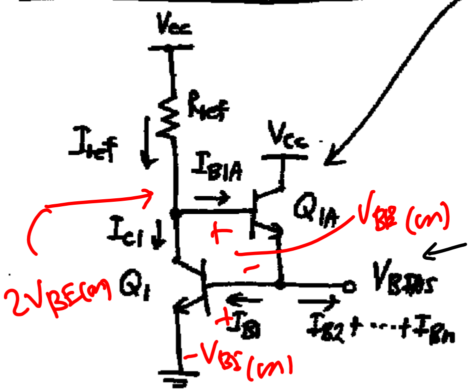
This was not the case for MOS!

How can one reduce the error?

To reduce the error term, use a

$\boxed{\text{Buffered } V_{BIAS} \text{ Generator}}$

Add a buffer Xsistor to attenuate base currents from Xsistor current sources.



This can now drive the base currents of many bipolar transistor current sources (i.e., active loads).

$$I_{ref} = I_{C1} + I_{B1A}$$

$$I_{B1A} = \frac{I_{B1}+I_{B2}+\cdots I_{Bn}}{\beta+1} = \frac{nI_{C1}}{\beta(\beta+1)}$$

[Assuming identical Xsistors]

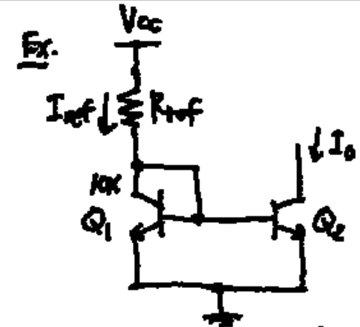
$$I_{ref} = I_{C1}\left(1+\frac{n}{\beta(\beta+1)}\right)$$

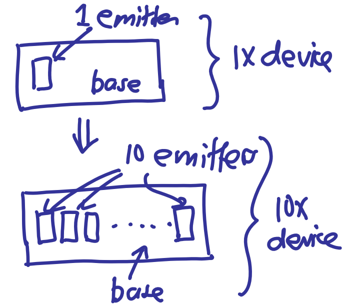
$$\rightarrow \boxed{I_o = I_{C2} = \frac{I_{ref}}{1+\frac{n}{\beta(\beta+1)}} \approx I_{ref}\left(1-\frac{n}{\beta^2}\right)}$$

Note: Now, $\boxed{I_{ref} = \dfrac{V_{CC}-2V_{BE(on)}}{R_{ref}}}$

Problem: For power savings reasons, oftentimes very small bias currents are needed, on the order of $5\mu A$. This might force too large an R_{ref} in the above bipolar V_{BIAS} generator.

Ex.





i.e., larger emitter area: Layout like this to get more accurate ratio.

If Q_1 is 10X larger than Q_2.

$$\therefore I_{C1} = 10 I_{C2} \rightarrow I_o \cong I_{ref}/10$$

$$\therefore I_o = \frac{(V_{CC}-V_{BE(on)})}{10R_{ref}} \rightarrow R_{ref} = \frac{V_{CC}-V_{BE(on)}}{10 I_o}$$

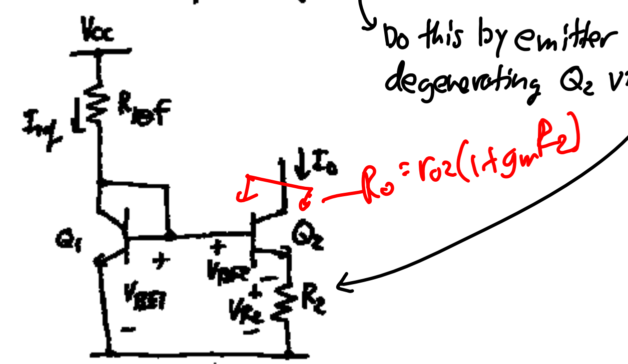
this helps to lower R_{ref}, but is it enough?

Ex. $I_o = 5\mu A$, $V_{CC} = 30V$

$R_{ref} \cong \frac{30}{5\mu} = \underline{600k\Omega}$ ← That's way too big! (Yes, there's only one of them on the chip, but this takes up too much space!)

The Low Current Solution: $\boxed{\text{Widlar Current Source}}$

⇒ scale $I_{C2} = I_o$ by reducing V_{BE2} (relative to V_{BE1}): Do this by emitter degenerating Q_2 via R_2



$$V_{BE1} = V_{BE2} + V_{R_2} = V_{BE2} + \frac{1}{\alpha} I_{C2} R_2 \approx V_{BE2} + I_{C2} R_2$$

$$I_{C2} R_2 = V_{BE1} - V_{BE2} = V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{C2}}{I_{S2}}$$

$$I_{C2} R_2 = V_T \ln \frac{I_{C1}}{I_{C2}}$$ [Assuming Q_1 & Q_2 are matched.]

$$\boxed{I_O R_2 = V_T \ln \frac{I_{ref}}{I_O}}$$

Rule of Thumb:

$V_{R_2} = I_{C2} R_2$	$I_{C2} = I_O$
18 mV	$\frac{1}{2} I_{ref}$
42 mV	$\frac{1}{5} I_{ref}$
60 mV	$\frac{1}{10} I_{ref}$
120 mV	$\frac{1}{100} I_{ref}$

Same example again

Ex. scale by 100X using Widlar source

$V_{BE1} - V_{BE2} = 120\text{mV} \rightarrow R_2 = \frac{120\text{mV}}{5\mu A} = \underline{24k\Omega}$

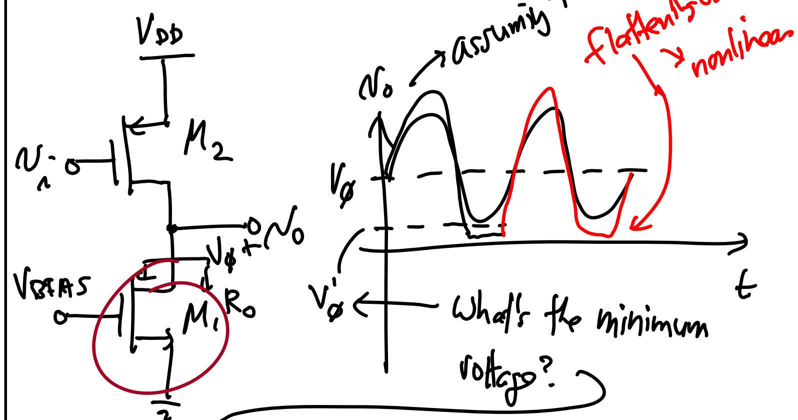
$I_{ref} = 500\mu A \rightarrow R_{ref} = \frac{30V}{500\mu A} = \underline{60k\Omega}$

More reasonable than 600kΩ before.
If want smaller, scale by 10X instead.

Another advantage of the Widlar: larger R_o ∴ a more ideal current source:

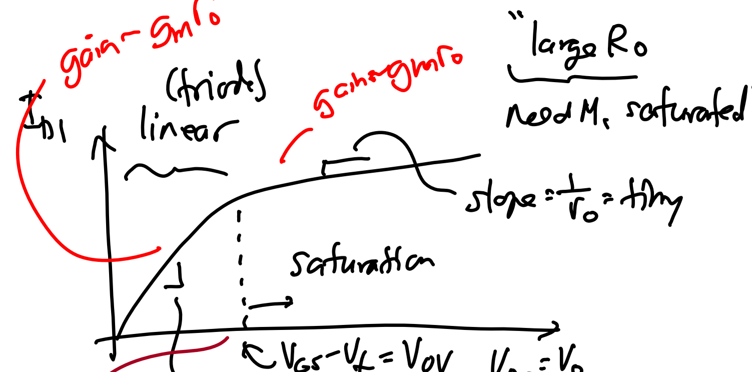
$R_o = r_{o2}(1 + g_{m2} R_2)$

Issue: Output Swing (Headroom)



Smallest V_ϕ' for which M_1 still behaves as a good current source.

"large R_o"
need M_1 saturated!



slope = large
R_o = small → we want to avoid the linear MOS region (triode)

*

$$V_{Dsat} = V_{GS1} - V_{t1} = V_{OV} = \Delta V = V_{OD}$$

overdrive voltage

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS1} - V_t)^2$$

$$V_{Dsat} = \Delta V = V_{OV} = V_{GS} - V_t = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}$$

$$V_{GS} = V_t + V_{OV}$$

(for long-channel devices)
(for short-channel it's different)

The min. voltage that still keeps M_1 as a good current source:

$$V_{omin} = V_{Dsat} = V_{OV}$$

$\therefore$ the output swing is:

$$V_{swing,pp} = V_{DD} - V_{Dsat1} - V_{Dsat2} = V_{DD} - 2V_{OV}$$

peak-to-peak