Issued: Thursday, Jan.24, 2013

Due (at 8 a.m.): Friday, Feb. 1, 2013, in the EE 140/240A HW box near 125 Cory.

1. Calculate the built-in potential, depletion layer depths, and maximum field in an abrupt pn junction in silicon with doping densities $N_A = 8 \times 10^{15}\ \text{atoms/cm}^3$ and $N_D = 10^{17}\ \text{atoms/cm}^3$. Assume that the edges of the depletion region are sharply defined.

(a) Assume a reverse bias of 4V.

(b) Repeat (a) for zero external bias and 0.4V forward bias.

2. Calculate the zero-bias junction capacitance for the example in Problem 1, and also calculate the value at 4V reverse bias and 0.4V forward bias. Assume a junction area of $2 \times 10^{-5}\ \text{cm}^2$.

3. Derive and sketch the complete small-signal equivalent circuit for a bipolar transistor biased so that $I_C = 0.2\text{mA}, V_{CB} = 3\text{V}, V_{CS} = 4\text{V}$. Device parameters are: $C_{je0} = 20\text{fF}, C_{\mu 0} = 10\text{fF}$, $C_{CS0} = 20\text{fF}$, $\beta_0 = 100, \tau_F = 15\text{ps}, \eta = 10^{-3}, r_b = 200\Omega$, $r_c = 100\Omega, r_{ex} = 4\Omega$, and $r_\mu = 5\beta_0 r_o$. Assume $\psi_0 = 0.55\text{V}$ for all junctions.

4. An NMOS transistor has parameters $W = 10\mu\text{m}, L = 1\mu\text{m}$, $k' = 190\frac{\mu\text{A}}{\text{V}^2}$, $\lambda = 0.024\text{V}^{-1}, t_{ox} = 80\dot{\text{A}}, \phi_f = 0.3\text{V}, V_{t0} = 0.6\text{V}$, and $N_A = 5 \times 10^{15}\text{cm}^{-3}$. Ignore velocity saturation effects.

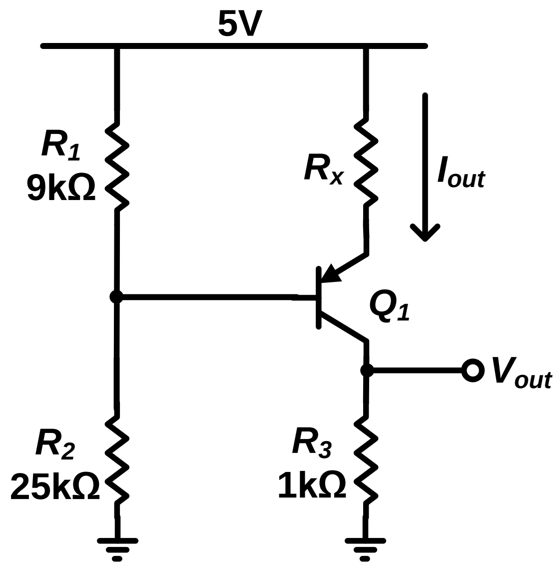
(a) Sketch the $I_D - V_{DS}$ characteristics for V_{DS} from 0 to 3V and $V_{GS} = 0.5\text{V}, 1.5\text{V}$ and 3V assume $V_{SB} = 0$.

(b) Sketch the $I_D - V_{GS}$ characteristics for $V_{DS} = 2\text{V}$ as V_{GS} varies from 0 to 2V with $V_{SB} = 0, 0.5\text{V}$, and 1V.

(c) Derive and sketch the *complete* small-signal equivalent circuit for the device with $V_{GS} = 1\text{V}, V_{DS} = 3\text{V}$ and $V_{SB} = 1\text{V}$. Use $\psi_0 = 0.7\text{V}, C_{sb0} = C_{db0} = 20\text{fF}$, and $C_{gb} = 5\text{fF}$. Overlap capacitance from gate to source and gate to drain is 2fF.

(d) Under the bias condition in (c), calculate the frequency of unity current gain of this device.

5. In the circuit shown below, find I_{out} and V_{out} for **(a)** $R_x = 4\text{k}\Omega$, **(b)** $R_x = 2\text{k}\Omega$, and **(c)** $R_x = 1\text{k}\Omega$. Assume $V_{BE(on)} = 0.7\text{V}, V_{CE(sat)} = 0.2\text{V}$, and $\beta \to \infty$.



6. Calculate the DC operating points including the current flowing through each branch and DC voltage at each node for the circuits shown:

$V_{DD} = V_{CC} = 5\text{V}, \beta_f = 100, V_A \to \infty, r_b = 0, V_{BE(on)} = 0.7\text{V}, V_{CE(sat)} = 0.2\text{V},$

$k_n' = 140\frac{\mu\text{A}}{\text{V}^2}, V_{tn} = 0.7\text{V}, k_p' = 40\frac{\mu\text{A}}{\text{V}^2}, V_{tp} = -0.8\text{V}, \lambda = 0$

$\left(\frac{W}{L}\right)_1 = \frac{10\mu\text{m}}{0.5\mu\text{m}}, \left(\frac{W}{L}\right)_2 = \frac{25\mu\text{m}}{0.5\mu\text{m}}, \left(\frac{W}{L}\right)_3 = \frac{10\mu\text{m}}{0.5\mu\text{m}}, \left(\frac{W}{L}\right)_4 = \frac{15\mu\text{m}}{0.5\mu\text{m}}$