PROBLEM SET #11

Issued: Thursday, Apr. 18, 2013

Due (at 8 a.m.): Friday, Apr. 26, 2013, in the EE 140/240A HW box near 125 Cory.

1. For the two-stage amplifier shown in Fig. PS11.1, assume $I_{Bias} = 20\mu A$, and the output voltage V_{out} is biased to 0V. Determine the size of MOS transistors and then compensate the amplifier to satisfy the following specifications:

  i) Low-frequency open-loop gain $\geq$ 90dB

  ii) Unity-gain bandwidth $\geq$ 3MHz

  iii) Phase margin $\geq 60^{o}$ for unity-gain feedback

  iv) Slew rate $\geq$ 4V/μs

  v) Peak-to-peak output swing $\geq$ 9.5V

You should size M_9 to move the zero introduced by the pole splitting to infinity.

<u>MOS parameters:</u>

$|V_{th}| = 0.7V$, $\mu_n = 700 cm^2/V\text{-}s$, $\mu_p = 350 cm^2/V\text{-}s$, $\lambda_n = 0.015V^{-1}$, $\lambda_p = 0.03V^{-1}$,

$L_{min} = 1\mu m$, $C_{ox} = 86.3 nF/cm^2$, $C_{ol} = 0.35 fF/\mu m$,

$C_{j0} = 0.15 fF/\mu m^2$, $C_{jsw0} = 1 fF/\mu m$, $m_j = 0.5$, $m_{jsw} = 0.5$, $\varphi_0 = 0.65V$.

Note: All of transistor dimensions should be larger than L_{min} and use Lambda design rule to determine the MOS parasitic capacitors, if needed.
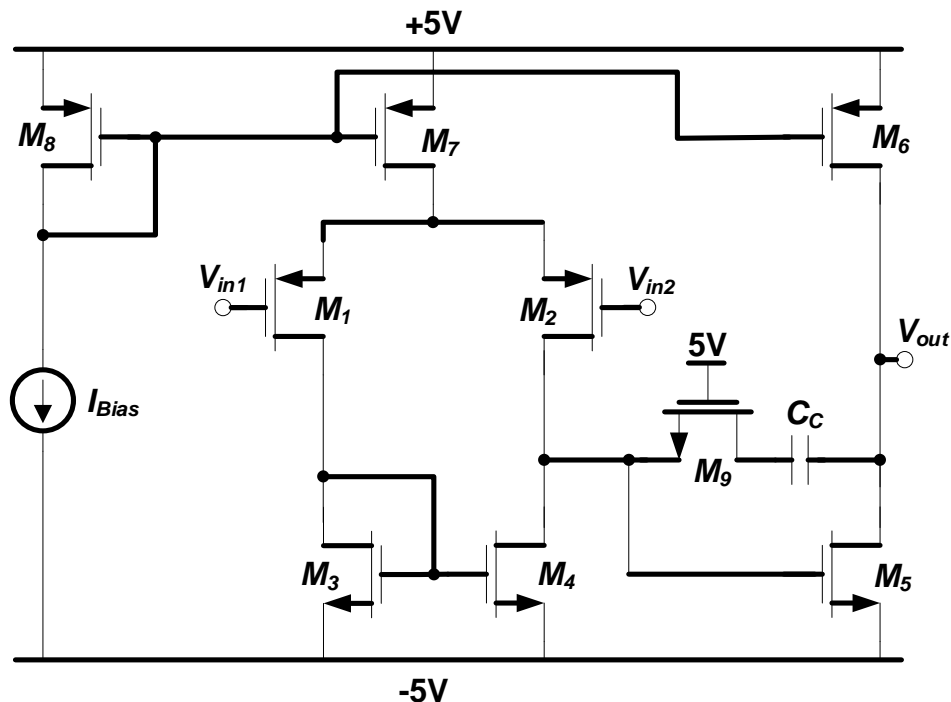

Figure PS11.1

2. In this problem, you will simulate using Hspice the op amp given in "ee140_hw11.sp." Its accompanying device model is given in "ee140_hw11_model.sp." For your convenience, the op amp circuit is pictorially shown below in Fig. PS11.2. Please give all gain values and ratios in dB.
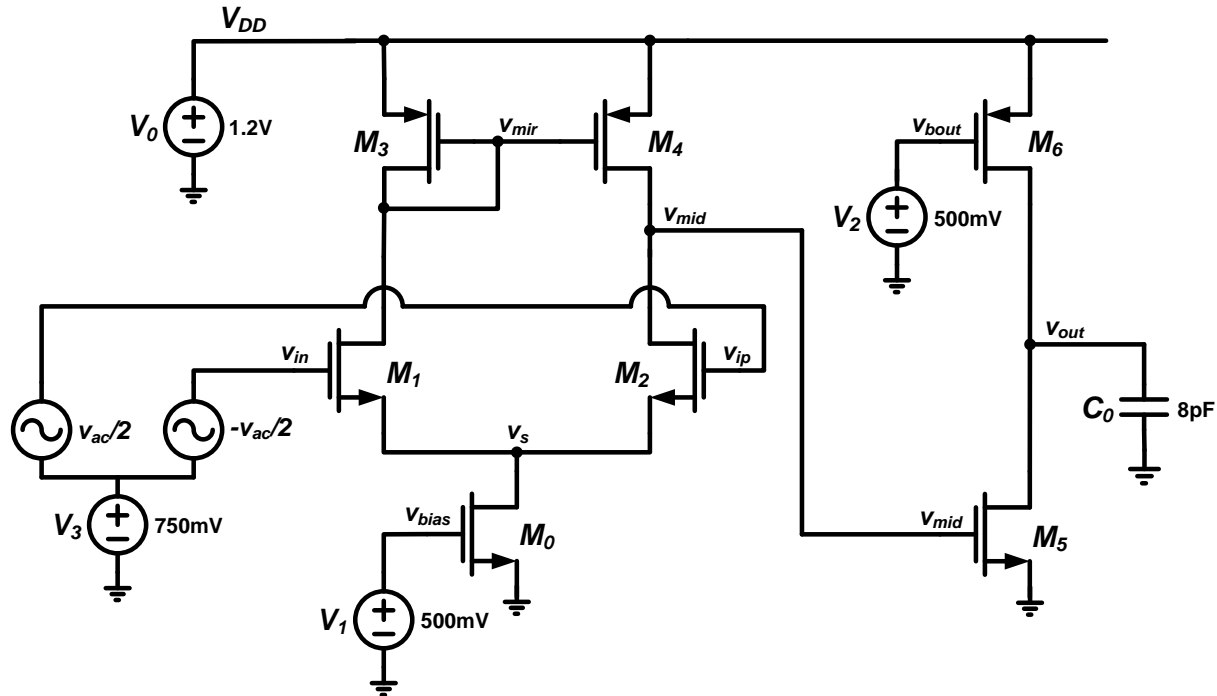

Figure PS11.2

a. Simulate the open loop AC gain and phase of the op amp. What is the op amp's gain at low frequencies? What is the op amp's unity gain frequency? What is the op amp's unity gain phase margin?

b. Simulate the common mode gain of the op amp by applying positive v_{ac} to both inputs. What is the op amp's common mode gain at low frequencies? What is the op amp's CMRR?

c. Simulate the power supply gain of the op amp:
  i.   Turn off the AC signal at the op amp's inputs.
  ii. Add an AC signal to the power supply voltage source *V0*.

  What is the op amp's power supply gain at low frequencies? What is the op amp's PSRR?

d. Simulate the output swing of the op amp using DC sweep analysis:
  i.   Sweep the DC voltage at one of the op amp's inputs around its bias point.
  ii. Take the derivative of the op amp's DC output voltage with respect to the swept input. Make sure there is enough resolution in your sweep to get an accurate result.

  For the purpose of this course (and your project), we will define the op amp's output swing range as the DC output voltages at which dV_{out}/dV_{in} becomes 1/10 the nominal differential gain (from part (a)). What is the op amp's output swing range?

e. Simulate the common mode input range of the op amp using DC sweep analysis:
  i.   Put the op amp into unity gain feedback.

ii.   Sweep the DC voltage of the op amp's input from 0 to VDD.

iii.   Take the derivative of the op amp's DC output voltage with respect to the swept input.

For the purpose of this course (and your project), we will define the op amp's input range as the DC input voltages at which dV_{out}/dV_{in} becomes 1/2 in unity gain feedback. What is the op amp's common mode input range?