EE 140 / EE 240A

PROBLEM SET #2

Issued: Thursday, Jan.31, 2013

Due (at 8 a.m.): Friday, Feb. 8, 2013, in the EE 140/240A HW box near 125 Cory.

1. Use inspection analysis to write expressions for the input resistance R_{in} , output resistance R_{out} , and gain v_{out}/v_{in} for each of the amplifiers in Fig. PS2.1. The expression should be in terms of the given elements and parameters of the small-signal equivalent circuits (i.e., g_m , r_π , r_o , etc) for the transistor used. For each circuit, assume that all the capacitors shown have infinite values.

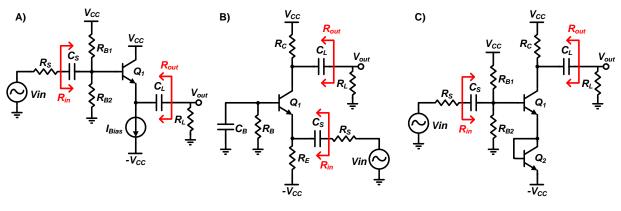
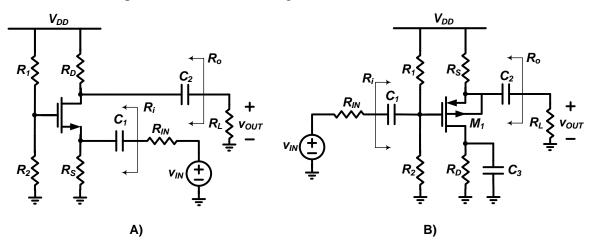


Fig. PS2.1

2. Use inspection analysis to write expressions for the input resistance R_i , output resistance R_o , and gain v_{out}/v_{in} for each of the amplifiers in Fig. PS2.2. The expressions should be in terms of the given elements and parameters of the small-signal equivalent circuits (i.e., g_m , g_{mb} , r_o , etc.) for the transistors used. For each circuit, assume that all capacitors shown have infinite values. Assume bulks are connected to ground and V_{DD} for NMOS and PMOS, respectively, unless otherwise specified in the circuit diagram.



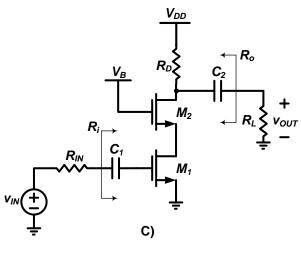


Fig. PS2.2

- **3.** Referring to the circuit shown in Fig. PS2.3, provide expressions in terms of given elements and transistor small-signal model parameters for:
 - (a) The equivalent small-signal resistance looking into the collector of Q_1 , R_{eq1} ; equivalent small-signal resistance looking into the emitter of Q_2 , R_{eq2} ; input resistance, R_{in} ; and output resistance, R_{out} .
 - (**b**) First stage gain, v_{o1}/v_{in} ; second stage gain, v_{out}/v_{o1} ; and total gain, v_{out}/v_{in} .

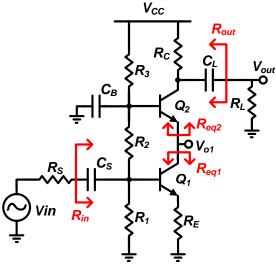


Fig. PS2.3

- **4.** Fig. PS2.5 depicts a "Darlington pair," where M_1 plays a role somewhat similar to a source follower driving Q_2 . In this problem do not neglect r_{o1} or r_{o2} .
 - (a) Determine the impedance seen looking into each terminal when all other terminals are tied to small-signal ground.

(b) Compute the transconductance of the pair, defined as $(i_{d1} + i_{c2})/v_{g1}$ when terminals 2 and 3 are tied to small-signal ground.

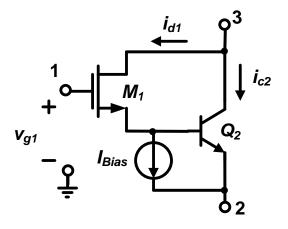


Fig. PS2.4