## PROBLEM SET \#3

Issued: Thursday, Feb.7, 2013
Due (at 8 a.m.): Friday, Feb. 15, 2013, in the EE 140/240A HW box near 125 Cory.

1. Referring to the multistage amplifier circuit shown in Fig. PS3.1:
(a) Calculate the DC operating points including the current flowing through each branch and DC voltage at each node.
(b) Calculate transistor small-signal parameters (i.e. $g_{m}, r_{\pi}, r_{o}, C_{\pi}, C_{\mu}, C_{g s}, C_{g d}$ )
(c) Provide expressions and calculate the numerical values for the input resistance, $R_{i n}$; output resistance, $R_{o u t}$; first stage gain, $v_{o 1} / v_{s}$; second stage gain, $v_{o 2} / v_{o 1}$; third stage gain, $v_{o u t} / v_{o 2}$ and total gain, $v_{o u} / v_{s}$.
(d) Estimate the low frequency cut-off $f_{L}$ and high frequency cut-off $f_{H}$ of the amplifier.

## BJT parameters:

$$
\beta=100, V_{A}=50 \mathrm{~V}, V_{B E(o n)}=0.7 \mathrm{~V}, V_{C E(S A T)}=0.2 \mathrm{~V}, \tau_{F}=150 \mathrm{ps}, C_{j e}=50 \mathrm{fF}, C_{\mu}=1 \mathrm{pF}, V_{T}=25 \mathrm{mV} .
$$

MOS parameters:

$$
V_{t h 0}=0.5 \mathrm{~V}, k^{\prime}=165.3 \mu \mathrm{~A} / \mathrm{V}^{2}, W / L=20 \mu \mathrm{~m} / 1 \mu \mathrm{~m}, \lambda=0.05 \mathrm{~V}^{-1}, C_{o x}=30 \mu \mathrm{~F} / \mathrm{cm}^{2}, C_{o l}=1 \mathrm{pF}, \gamma=0 .
$$



Fig. PS3. 1
2. For the small-signal circuits shown in Fig. PS3.2, assume all transistors are identical and have the following parameters:
$I_{D}=2 \mathrm{~mA}, W=50 \mu \mathrm{~m}, L_{d r w n}=130 \mathrm{~nm}, L_{d}=15 \mathrm{~nm}, X_{d}=0, k_{p}{ }^{\prime}=200 \mu \mathrm{~A} / \mathrm{V}^{2}, \gamma=0, \lambda=0$, $C_{o x}=15 \mathrm{fF} / \mathrm{mm}^{2}, C_{s b}=C_{d b}=0$.

Given $R_{S}=500 \Omega, R_{L}=1 \mathrm{k} \Omega$, and $C_{L}=50 \mathrm{fF}$ :
(a) Calculate the mid-band, small-signal voltage gain $v_{o} / v_{i}$ for each circuit.
(b) Calculate and compare the high 3-dB cutoff frequencies of the two circuits.


Fig. PS3. 2
3. For the both circuits depicted in PS3.3, calculate the input impedance, output impedance, and voltage gain, $v_{\text {out }} / v_{i n}$. Assume $\beta=100$ and $V_{A}=50 \mathrm{~V}$. Repeat assuming $V_{A}=\infty$.


Fig. PS3. 3
4. Design the common-base stage shown in Fig. PS3.4 for a voltage gain of 20 and an input impedance of $50 \Omega$ using a transistor with $\beta=100$ and $V_{A}=20 \mathrm{~V}$. Assume a voltage drop of $10 V_{T}=260 \mathrm{mV}$ across $R_{E}$ so that this resistor does not affect the input impedance significantly. Also, assume the current flowing through $R_{l}$ is approximately 10 times the base current, and the lowest frequency of interest is 200 Hz .


Fig. PS3.4

