## **PROBLEM SET #4**

Issued: Thursday, Feb.14, 2013

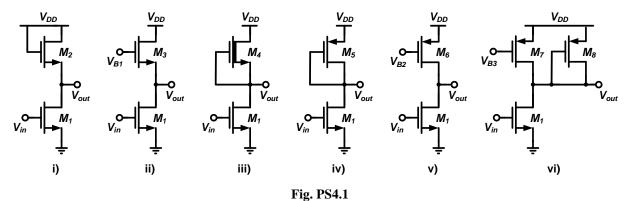
Due (at 8 a.m.): Friday, Feb. 22, 2013, in the EE 140/240A HW box near 125 Cory.

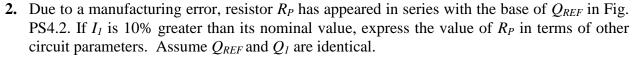
- 1. Fig. PS4.1 shows different active loads being used in analog circuits.
  - (a) Calculate the DC operating points including the current flowing through each branch and DC voltage at each node and transistor small-signal parameters (i.e.  $g_{m}$ ,  $r_o$ ,  $C_{gs}$ ,  $C_{gd}$ )
  - (b) Provide expressions and calculate the numerical values for the output resistance,  $R_{out}$ ; and gain,  $v_{out}/v_{in}$ .
  - (c) Estimate the high-frequency cut-off  $f_H$  of the amplifiers.

MOS parameters:

$$V_{GSI}=1V$$
,  $/V_{th}/=0.5V$ ,  $k_n = 200\mu A/V^2$ ,  $k_p = 100\mu A/V^2$ ,  $\lambda = 0.05V^{-1}$ ,  $V_{DD}=3V$ ,  $V_{BI}=2.7V$ ,  
 $V_{B2}=V_{B3}=1.5V$ ,  $C_{ox}=4fF/\mu m^2$ ,  $C_{ol}=3fF$ ,  $C_{sb}=C_{db}=5fF$ ;  
 $(W/L)_1=10\mu m/0.25\mu m$ ,  $(W/L)_{2,3}=2.5\mu m/0.25\mu m$ ,  $(W/L)_4=10\mu m/0.25\mu m$ ;  
 $(W/L)_{5,6}=5\mu m/0.25\mu m$ ,  $(W/L)_7=4.5\mu m/0.25\mu m$ ,  $(W/L)_8=0.5\mu m/0.25\mu m$ .

Note that the active load in circuit (iii) is depletion-mode NMOS and hence its threshold voltage is negative (i.e.  $V_{th4}$ =-0.5V).





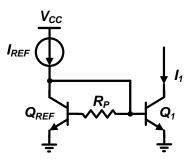


Fig. PS4.2

3. Determine the value of  $R_P$  in the circuit of Fig. PS4.3 such that  $I_I = I_{REF}/2$ . With this choice of  $R_p$ , does  $I_I$  change if the threshold voltage of both transistors increases by  $\Delta V$ ?

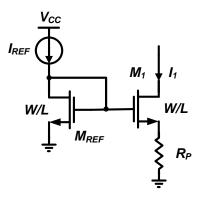


Fig. PS4.3

- **4.** Fig. PS4.4 depicts a simple amplifier circuit using active load. Assume that the output voltage is set at 1V.
  - (a) Calculate the DC operating points including the current flowing through each branch and DC voltage at each node.
  - (b) Calculate transistor small-signal parameters (i.e.  $g_{m}$ ,  $g_{mb}$ ,  $r_o$ ,  $C_{gs}$ ,  $C_{gd}$ ).
  - (c) Provide expressions and calculate the numerical values for the output resistance,  $R_{out}$ ; and gain,  $v_{out}/v_{in}$ .
  - (d) Estimate the high-frequency cut-off  $f_H$  of the amplifier.

MOS parameters: (for both NMOS and PMOS, unless otherwise stated)

 $/V_{th} = 0.5 \text{V}, k_n = 200 \mu \text{A}/\text{V}^2, k_p = 100 \mu \text{A}/\text{V}^2, V_{DD} = 2.5 \text{V},$ 

 $\lambda = 0.05 \text{V}^{-1}$ ,  $\chi = 0.1$ ,  $C_{ox} = 5 \text{fF}/\mu\text{m}^2$ ,  $C_{ol} = 3 \text{fF}$ ,  $C_{sb} = C_{db} = 5 \text{fF}$ 

 $(W/L)_1 = 2.25 \mu m/0.25 \mu m, (W/L)_2 = 4.5 \mu m/0.25 \mu m, (W/L)_{3,4} = 3.75 \mu m/0.25 \mu m,$ 

 $(W/L)_{5,6}=11.25\mu m/0.25\mu m, (W/L)_7=37.5\mu m/0.25\mu m, (W/L)_8=7.5\mu m/0.25\mu m,$ 

 $(W/L)_9 = 6.25 \mu m/0.25 \mu m, (W/L)_{10} = 12.5 \mu m/0.25 \mu m, (W/L)_{11} = 11.25 \mu m/0.25 \mu m.$ 

<u>*Hint*</u>: Since the current into the transistor  $M_1$  is fixed by the ideal current source, there is no change at its gate voltage, i.e. it is *ac* ground. You can assume the same is true for  $M_3$  and  $M_4$ , too.

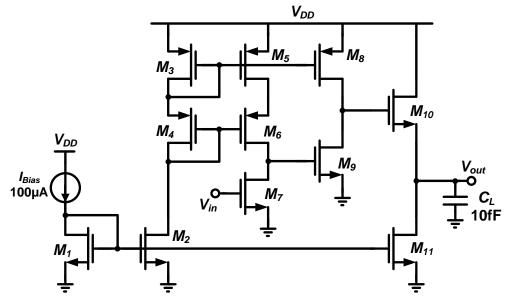


Fig. PS4.4