PROBLEM SET #5

Issued: Thursday, Feb.21, 2013

Due (at 8 a.m.): Friday, Mar. 1, 2013, in the EE 140/240A HW box near 125 Cory.

1. In the circuit shown in Fig. PS5.1, a source follower using a wide transistor M_4 and a small bias current is inserted in series with the gate of M_3 so as to bias M_2 at the edge of saturation. Assuming M_0 - M_3 are identical and $\lambda \neq 0$, estimate the mismatch between I_{out} and I_{REF} if:

(a) $\gamma = 0$

(b) $\gamma \neq 0$

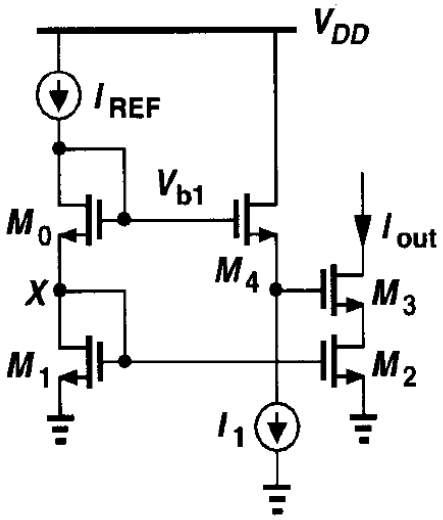

Fig. PS5.1

2. Compute the error, defined as $(I_{REF}-I_{Copy})/I_{REF}$, in I_{copy1} and I_{copy2} for both circuits in Fig. PS5.2. Assume $\beta = 20$.

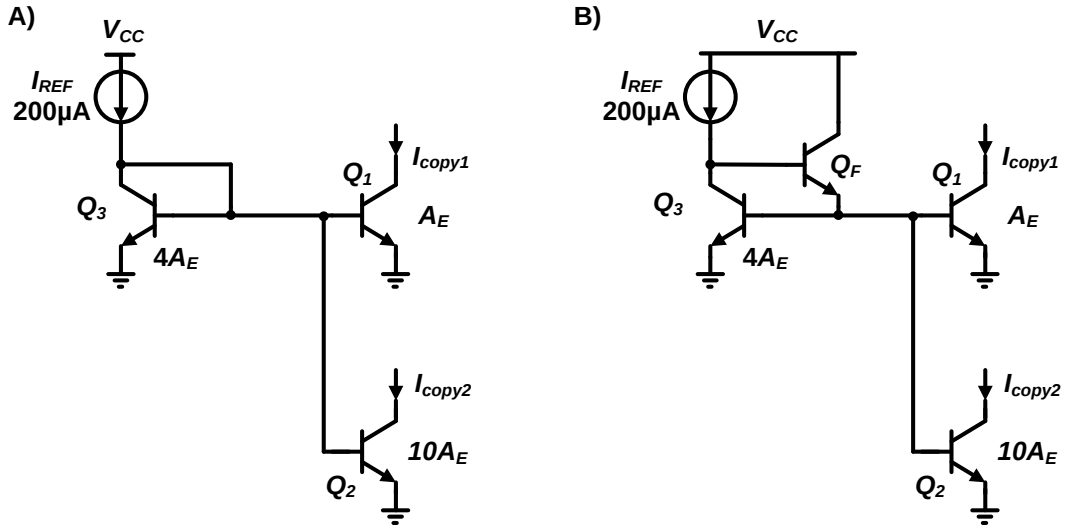

Fig. PS5.2

3. Fig. PS5.3(A) shows a common source amplifier that is biased using a current mirror. Assume that R_B and C_B have infinite values, and that the transistors have the following parameters:

L = 120 nm, V_{th0} = 0.5 V, k_n' = 200 μA/V^2, γ = 0.

Given V_{DD} = 1.5 V, W_1 = 3 μm, I_{REF} = 100 μA, and R_L = 1 kΩ:

(a) Assuming λ = 0, size M_2 (i.e. find W_2) so that the amplifier has a mid-band, small-signal voltage gain v_o/v_i = 5. What is the bias current I_{D2} in this case?

(b) Keep the same size for M_2 that you found in part (a), but now let λ = 0.2 V^{-1}. What is the new bias current I_{D2}? What is the new small-signal voltage gain? Explain the source of mismatch with your results from part (a).

(c) In order to more accurately control the bias current, we could add a cascode device to the amplifier, as shown in Fig. PS5.3(B). Find the bias voltage V_B that will make the bias current I_{D2} match what was found in part (a) exactly. Assume $(W/L)_3 = (W/L)_2$, and λ = 0.2 V^{-1} still.

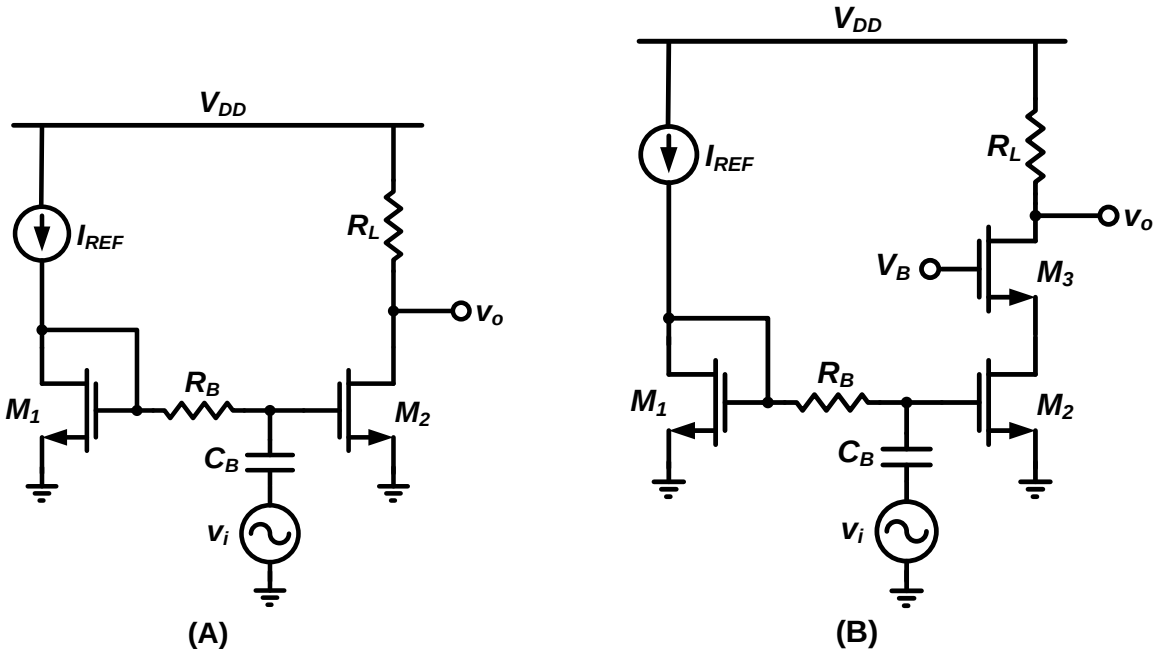

Fig. PS5.3

4. Fig. PS5.4 depicts a self-biasing V_t reference circuit which is capable of providing a current reference independent of biasing voltage.

(a) Provide expressions for the DC output current I_{OUT} and biasing currents I_{BIAS1} and I_{BIAS2} in terms of circuit elements and transistor parameters and calculate numerical values. Ignore body effect and channel length modulation.

(b) Calculate the ratio of small-signal variations in I_{OUT} to small-signal variations in V_{DD} at low frequencies. Ignore the body effect but include finite transistor r_o in this calculation.

MOS parameters:

$|V_{th}|$=0.5V, k_n'=200μA/V^2, k_p'=100μA/V^2, λ=0.05V^{-1}, V_{DD}=3V, R=1.75kΩ,

$(W/L)_1$=12.5μm/0.25μm, $(W/L)_2$=6.25μm/0.25μm, $(W/L)_3$=31.25μm/0.25μm,

$(W/L)_4$=6.25μm/0.25μm, $(W/L)_5$=12.5μm/0.25μm, $(W/L)_6$=15.5μm/0.25μm.

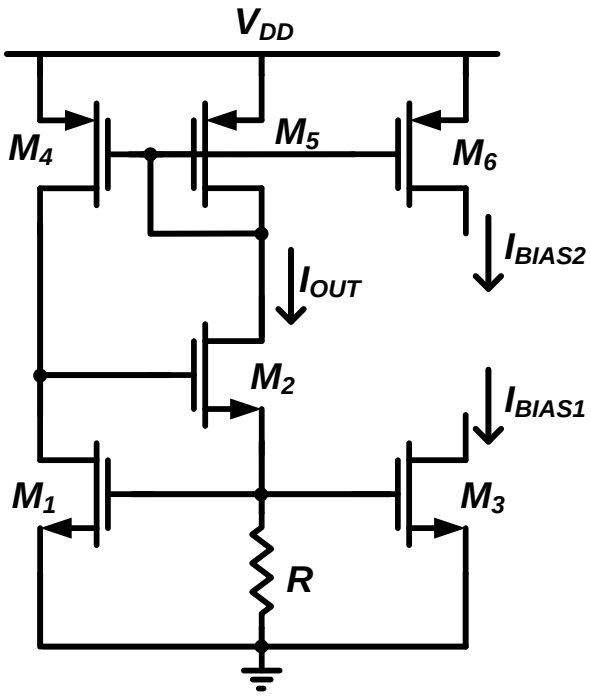

Fig. PS5.4