PROBLEM SET #7

Issued: Thursday, Mar. 7, 2013

Due (at 8 a.m.): Friday, Mar. 15, 2013, in the EE 140/240A HW box near 125 Cory.

1. You are given the op amp-based amplifier circuit shown in Fig. PS7.1.

(a) Assuming the op amp is ideal, derive the expression and find a numerical value for the closed-loop gain of the circuit.

(b) Now assume the op amp has a gain of 60dB, -3dB bandwidth of 10MHz, input resistance of 100kΩ, and output resistance of 100Ω. Find numerical values for the closed-loop gain and closed-loop frequency response of the circuit. What is the fractional error in closed-loop caused by the non-idealities?

(c) Assuming again that the op amp is ideal, what is the expected output for V_{in} = 1mV?

(d) How does your answer to part (c) change if the amplifier has 0.1mV of input-equivalent offset voltage and 0.5μA of input bias current?

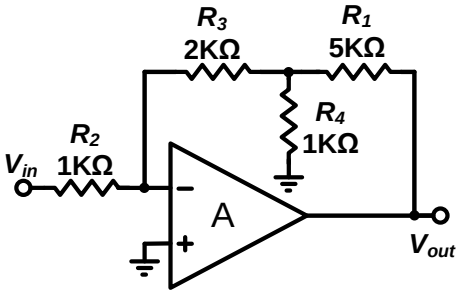

Fig. PS7.1

2. Consider a two-pole op amp with a dc gain of 40dB, and with its poles at $\omega_{p1}=\omega_0$ and $\omega_{p2}=100\times\omega_0$. The input and output impedances of the op amp are large and small enough, respectively, to be negligible. Using this op amp, we construct the feedback systems shown in Fig. PS7.2.

For each system in Fig. PS7.2, find the transfer function $V_{out}(s)/V_{in}(s)$ and sketch the Bode plot. You may make reasonable approximations in your sketches, but do label all gain, pole/zero locations, and slopes. For part (c), assume $1/(RC) << \omega_0/100$.

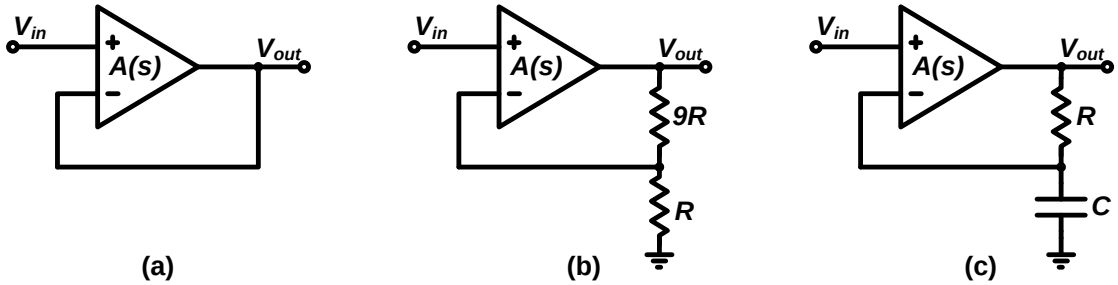

Fig. PS7.2

3. For the amplifiers shown in Fig. PS7.3, provide expressions for the gain, output resistance and high-frequency cut-off f_H, in terms of transistors small-signal parameters (i.e. g_m, g_{mb}, r_o, C_π, C_μ, C_{cs}, C_{gs}, C_{gd}, C_{db}, C_{sb}) for common-mode and differential-mode input.

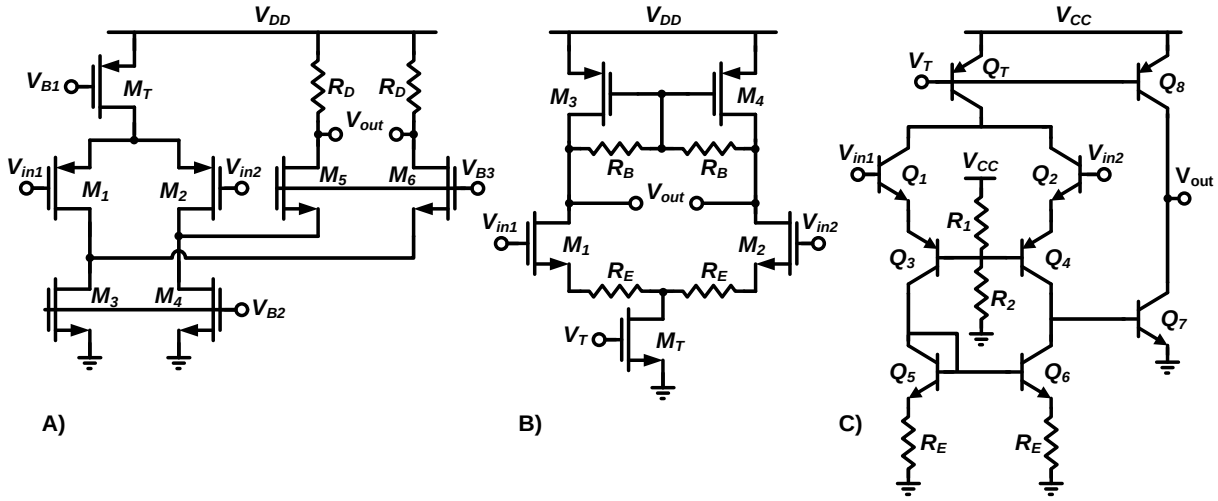

Fig. PS7.3

4. For the amplifier shown in Fig. PS7.4, provide expressions and calculate numerical values for the gain, output resistance and high-frequency cut-off f_H.

MOS parameters:

$|V_{th}| = 0.5\text{V}$, $k_n' = 200\mu\text{A/V}^2$, $k_p' = 100\mu\text{A/V}^2$, $\lambda = 0.05\text{V}^{-1}$, $V_{DD} = 3\text{V}$,

$C_{ox} = 4\text{fF/}\mu\text{m}^2$, $C_{ol} = 3\text{fF}$, $C_{sb} = C_{db} = 0.5\text{fF}$,

$(W/L)_B = 0.5\mu\text{m}/0.25\mu\text{m}$, $(W/L)_T = 5\mu\text{m}/0.25\mu\text{m}$, $(W/L)_{1,2} = 12.5\mu\text{m}/0.25\mu\text{m}$,

$(W/L)_{3,4} = 5\mu\text{m}/0.25\mu\text{m}$, $(W/L)_5 = 10\mu\text{m}/0.25\mu\text{m}$, $(W/L)_6 = 4.5\mu\text{m}/0.25\ \mu\text{m}$,

Assume that the input node is biased at 0V and the output DC voltage is set at 0V, too.

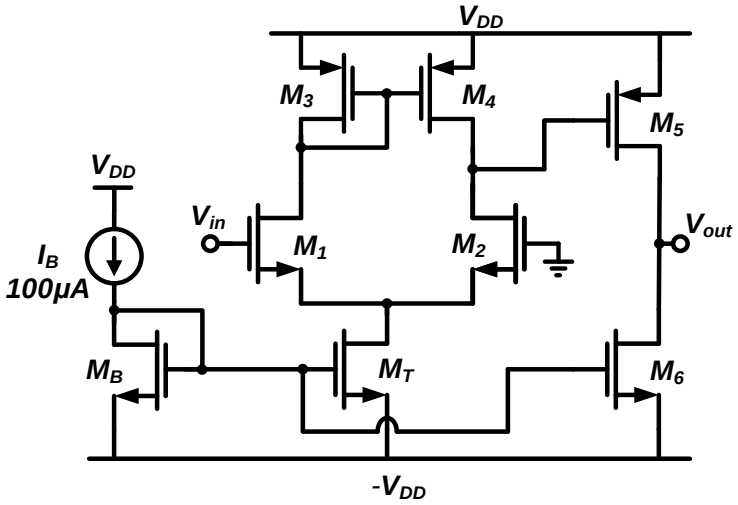

Fig. PS7.4

5. Determine the input offset voltage of the source-coupled pair in Fig. PS7.5, for which I_{TAIL}=50μA and L=1μm. Use the process parameters given in Table 2.4 of your Gray & Meyer textbook. Assume that the worst-case W/L mismatch is 2 percent and the device thresholds are identical. Also assume that X_d=0, $R_{TAIL}\rightarrow\infty$, and the load resistors are identical.

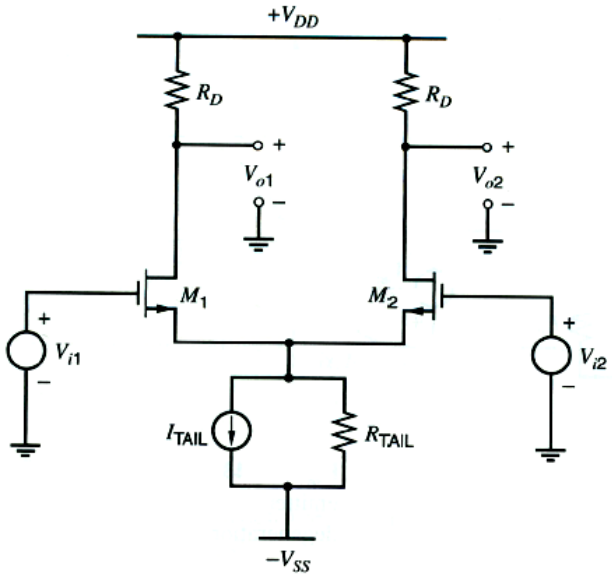

Fig. PS7.5