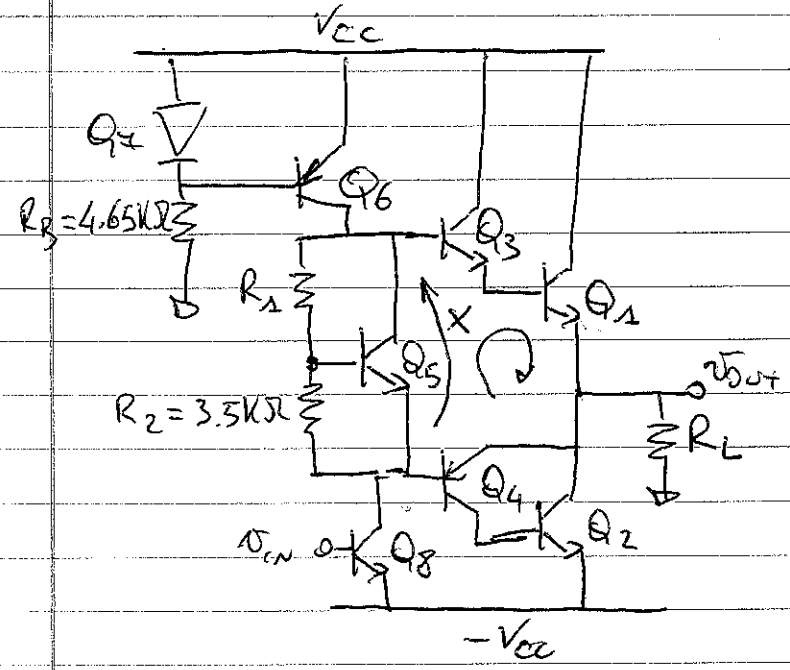
EE140/EE240A

Discussion 10

Problem 1



$V_{BE}(on) = 0.7V$

$\beta_{1,2} = 20$

$\beta_{3,8} = 100$

$V_A = 50V$

$V_{CE_{sat}} = 0.2V$

$V_{CC} = 10V$

a) Find R_1 to have no dead zone

We recognize class A/B operation from the presence of Q_2-Q_4 at any time, only one of those transistors will be on. If we want no deadzone, we need to make sure that all transistors operate at the edge of turn-on.

① KVL @ 1: $X = V_{BE_3} + V_{BE_1} + V_{EB_4} = 3 \cdot 0.7V = 2.1V$

② Resistive divider Ohm's law $\frac{X}{R_2 + R_1} = \frac{V_{BE5}}{R_2} \Rightarrow X = \left(\frac{R_1}{R_2} + 1\right) \cdot 0.7V$

where we ignored the base current in Q_5

$\Rightarrow$ combining 1 & 2: $R_1 = 2R_2 = 7K\Omega$

b) Find maximum amplitude of the output voltage $v_{OUT} = v_M \sin(\omega t)$ for $R_L = 100\,\Omega$

There are two limiting factors for the output voltage
1) Supply clipping or Transistor operating region
2) Current capabilities

We need to compute both and see which ~~one~~ is the limiting one.

- Voltage clipping (positive output cycle)

Q_1 in saturation $V_{M_{MAX}} = V_{CC} - V_{CESAT_1} = 9.8V$

Q_3 " " $V_{M_{MAX}} = V_{CC} - V_{CESAT_3} - V_{BE_1} = 9.1V$

Q_6 " " $V_{M_{MAX}} = V_{CC} - V_{CESAT_6} - V_{BE_3} - V_{BE_1} = 8.4V$

For now our limit is $V_{M_{MAX}} \leq 8.4V$

Negative output cycle

Q_2 in saturation $V_M = -V_{CC} + V_{CESAT_2} = -9.8V$

Q_4 " " $V_M = -V_{CC} + V_{BE_2} + V_{CESAT_4} = -9.1V$

Q_8 " " $V_M = -V_{CC} + V_{CESAT_8} + V_{BE_4} = -9.1V$

So the limit is still $V_{M_{MAX}} \leq 8.4V$

- Current limit

Positive output cycle

Assume Q_5 has small I_C (just at the edge of F.A)

$I_{Q7} = \frac{V_{CC} - V_{BE}}{R_B} = 2mA$ Ignore $I_{B,Q6}$

$V_{BE7} = V_{BE6} \Rightarrow I_{Q6} = 2mA$

The current in R_1 & R_2 is $I_{R_2} = \frac{V_{BES}}{R_2} = 0.2mA$

$\Rightarrow I_{BQ3} = I_{Q6} - I_{R_2} = 1.8mA$

Through beta multiplication:

$v_{H_{MAX}} = I_{BQ3} \cdot \beta_3 \cdot \beta_1 \cdot R_L = 360V$!

In reality, some current will flow in Q_5 but the circuit is not going to be current limited for the chosen R_L thanks to the β-multiplication

Negative output cycle

There is no bias network limiting the bottom port current capabilities, so no limit in current (until the current hits the thermal limits of the devices)

$\Rightarrow V_{H_{MAX}} = 8.4V$

c) Max P_{LOAD} for $R_L = 500\,\Omega$ and efficiency η

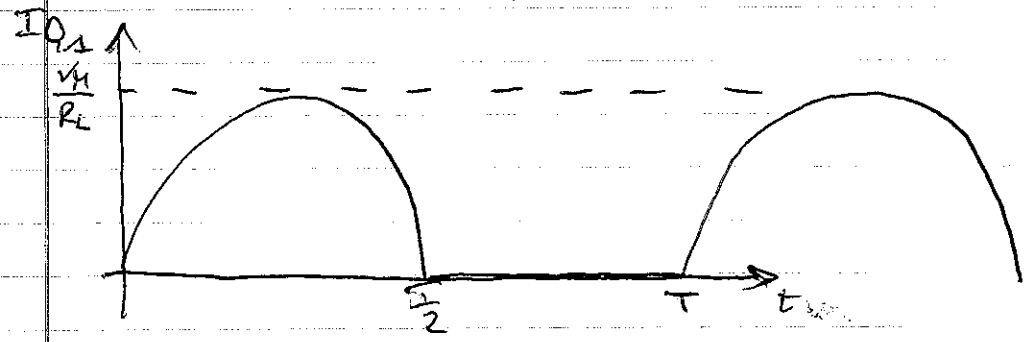
$$P_{LOAD}(t) = \frac{V_M^2 \sin^2 \omega t}{R_L} \rightarrow \hat{P}_{L_{AVE}} = \frac{1}{2}\frac{\hat{v}_M^2}{R_L} = 352.8\ mW$$

with $V_M = 8.4\,V$

For the efficiency we need to compute the current provided by the supply

Q_6 & Q_7 have constant current
Q_1 & Q_3 are on only the positive output cycle.

$$I_{Q_1} + I_{Q_3} = \left(1 + \frac{1}{\beta_1}\right)\frac{v_M}{\pi R_L}$$



$$\hat{I}_{Q_1} = \frac{1}{T}\int_0^T I_{Q_1}\,dt = \frac{1}{T}\int_0^{\frac{T}{2}} \frac{v_M}{R_L}\sin\omega t\,dt = \frac{v_M}{\pi R_L}$$

Q_2 is on only on the negative cycle: $I_{Q_2} = \frac{V_M}{\pi R_L}$

Q_8 is on all the time with a DC current of $I_{Q_8} = 2mA$ (from Q_6) and a sinusoid superimposed which would cancel out by averaging.

From positive supply $\overline{I}^{+}_{V_{CC}} = \overline{I}_{Q_7} + \overline{I}_{Q_6} + \overline{I}_{Q_3} + \overline{I}_{Q_1} = 4\,mA + \left(1 + \frac{1}{\beta_1}\right)\frac{V_M}{\pi R_L}$

From negative supply $\overline{I}^{-}_{V_{CC}} = \overline{I}_{Q_8} + \overline{I}_{Q_2} = 2\,mA + \frac{V_M}{\pi R_L}$

$$\Rightarrow P_{SUPPLY} \cong V_{CC}\left[3 I_{Q6} + 2\frac{V_M}{\pi R_L}\right] = 594.7\,mW \text{ @ } V_M = 8.4V$$

$$\Rightarrow \eta = \frac{P_{LOAD}}{P_{SUPPLY}} = 59.3\%$$

d) Find maximum average power in Q_1

In the negative output cycle the power is null.
In the positive output cycle:

$$\overline{P}_{M_1} = \frac{1}{T}\int_0^{\frac{T}{2}} \frac{V_M \sin(\omega t)}{R_L} \cdot \left(V_{CC} - V_M \sin \omega t\right) dt$$

$$= \frac{1}{T}\int_0^{\frac{T}{2}} \frac{V_M V_{CC}}{R_L} \sin \omega t \, dt - \frac{1}{T}\int_0^{\frac{T}{2}} \frac{V_M^2}{R_L} \sin^2 \omega t \, dt$$

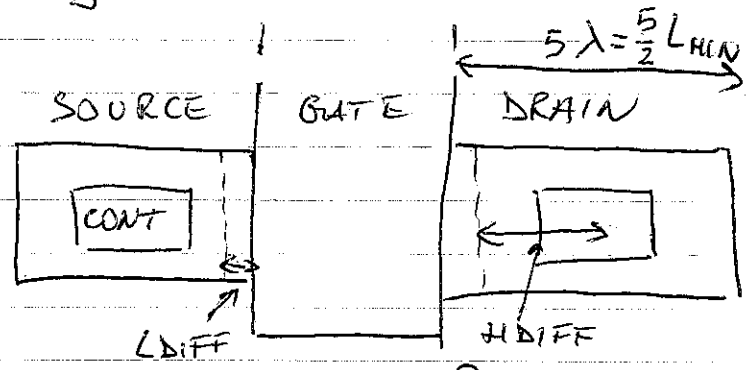
$$= \frac{V_{CC} V_M}{\pi R_L} - \frac{V_M^2}{4 R_L} = 90.98\,mW \text{ @ } V_M = 8.4V$$

2) LAMBDA RULES

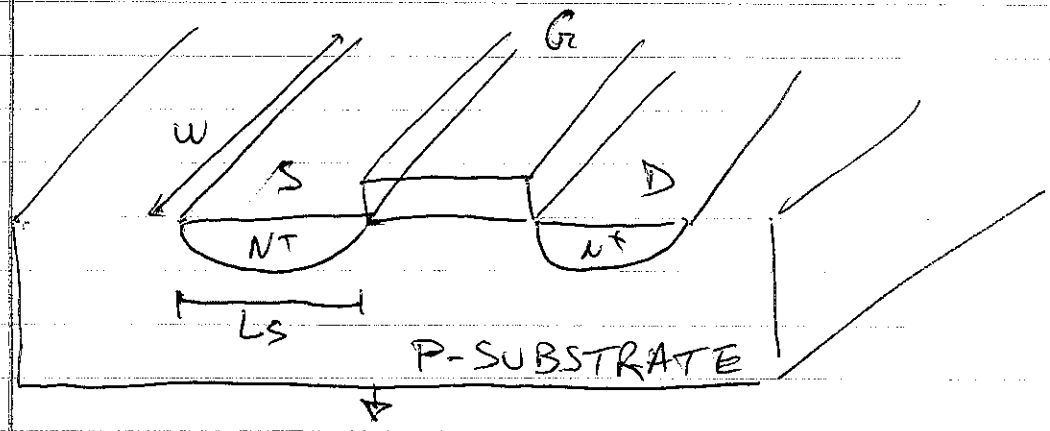
Need for "contract" between design and process engineers on what is possible to fabricate on silicon
- → spacing rules
- → minimum width rules

All rules defined as a multiple of parameter λ.
Then, typical minimum line width is set to 2λ

Advantages: easy
Disadvantage: too conservative



$L_{DIFF} = \lambda = 65\,nm$
$H_{DIFF} = 2\lambda = 130\,nm$
} In our 130 nm process



The PN junction at the source and drain is reversed-biased.

This creates a depletion region around the junction, which acts as a parasitic capacitive component C_{DB} & C_{SB}!

For a reverse-biased junction:

$$C_{JUNCTION} = \frac{C_{JUNCTION,0}}{\sqrt{1 - \frac{V_\Delta}{\psi_0}}} \quad \text{with } \psi_0 = \text{built-in potential}$$

$$C_{JUNCTION,0} = C_{BOTTOM_0} + C_{SIDE\text{-}WALL_0}$$

$$= C_{J0} \cdot AREA + C_{JSW_0} \cdot PERIMETER$$

$$= C_{J0} \cdot (5\lambda \cdot W) + C_{JSW_0} \cdot (10\lambda + W)$$