EE 140/240A **ANALOG INTEGRATED CIRCUITS** **SPRING 2014**

Vladimir Stojanović

INFORMATION ABOUT THE FINAL EXAM

Office hours for the RRR week:

Prof. Stojanovic	MWF 2-3pm in Cory 513
Alberto Puggelli	M 6-8pm, F 4-6pm
Filip Maksimovic	W 3-6pm

Date of exam: Tuesday, May 13, 8-11 am. (sharp)

Place: 247 Cory

General information:

The exam will be closed book, but you will be allowed one 8.5″×11″ sheet on which you can write anything you would like on both sides of the paper. Bring a calculator to the exam. You will be provided with exam sheets with enough space to put all your work on these sheets. You should show and include all your work on the exam sheets.

During the exam, make appropriate engineering decisions and approximations in order to simplify your analyses so that you can do the problems quickly and with fewer errors. In other words, the use of inspection analysis (where applicable) is encouraged.

Material to be covered:

Reading in Gray & Meyer, class lecture notes, handouts, and homeworks. The exam is meant to include all material covered in the class. You might want to pay more attention to the following areas:

1. Multiple transistor amplifier circuits, using BJT and/or MOS transistors, including cascodes and cascades, either actively or passively loaded. Be able to determine bias points, gain, impedance, and frequency response.

2. Derivation of input offset voltages and currents for (possibly unfamiliar) circuits.

3. Transistor bias generators and current sources, including ability to determine output current, output resistance, and output swing for a circuit using a given (possibly unfamiliar) current source. You should also be able to design a current source to insure a given swing for a given biased amplifier circuit.

4. Biasing and small-signal analysis (for gain, impedance, and dominant pole) of single and two-stage op amps.

5. Differential pair amplifiers, either actively or passively loaded, including such concepts as biasing, differential-mode gain, common-mode gain, CMRR, half-circuits, and various impedances.

6. Compensation design and techniques, including an understanding of feedback concepts (e.g., closed-loop gain, loop transmission, etc. …), phase margin, narrowbanding, and pole splitting.

7. Basics of output stage design, including Class A and Class B designs.

8. Analysis of multi-stage BJT and MOS amplifiers with feedback (loop gain, return-ratios, closed-loop gain, input and output impedances). 2-port and return-ratio analysis, Blackman formula. Understanding of feedback connection types, feedback loading, the four general amplifier types and their ideal characteristics.

9. Design of operational amplifier circuits, in either bipolar or MOS technology (or both), including biasing and all aspects of small-signal and large-signal performance. Be able to determine common-mode input range, power supply rejection ratio, common-mode rejection ratio, slew rate, phase margin, input offset voltage, as well as gain, frequency, and impedances.

Although this exam is centered upon the above concepts, you are also responsible for understanding the required prerequisite background, such as small-signal analysis, Bode plots, device models, etc. Work fast on the exam, making reasonable approximations as necessary to simply problems. (Remember, the ability to simplify a difficult problem is one of the keys to successful circuit analysis.)