## Homework 10

Due: Monday, April 21, 2014 at 1pm

## This is an individual assignment!

## PROBLEM 1 (20pts):

Consider the class AB output stage depicted in Figure 1. Assume that the DC value of the input signal has been adjusted such that output DC voltage is set at zero.
(a) Find the DC biasing points of the circuit at rest (when there is no $a c$ signal at the input).

From now on, assume the circuit is in the steady state with $\operatorname{vin} \sin \left(2 \pi f_{0} t\right)$ as the input signal and $v m \sin \left(2 \pi f_{0} t\right)$ as the output signal.
(b) Find the maximum value of $v_{m}$ for $R_{L}=100 \Omega$ and $R_{L}=50 \Omega$, such that there is no clipping in the output waveform.
(c) Find the maximum output power delivered to $100 \Omega$ and $50 \Omega$ loads and calculate the efficiency of the output stage in each case (include all the elements).
(d) Find the maximum average power dissipated in transistors $Q_{1,2}$.
(e) Find the optimum value of $R_{L}$ that maximizes the efficiency of the output stage.

BJT parameters:
$Q 1-2: I_{S I}=I_{S 2}=1 \times 10^{-13} \mathrm{~A}, \beta_{n p n}=50, \beta_{p n p}=30, V_{A}=50 \mathrm{~V}, V_{C E(s a t)}=0.2 \mathrm{~V}$, Q3-4: $I_{S 3}=I_{S 4}=5 \times 10^{-14} \mathrm{~A}$,
Q5-7: $V_{B E(o n)}=0.7 \mathrm{~V}, \beta=100, V_{A}=50 \mathrm{~V}, V_{C E(\text { sat })}=0.2 \mathrm{~V}$,
$V_{C C}=10 \mathrm{~V}, V_{T}=25 \mathrm{mV}$.


Figure 1

## PROBLEM 2 (20pts):

Consider a class B output stage depicted in Figure 2(a). Assume $V_{C C}=10 \mathrm{~V}$, and both transistors have the same $\left|V_{t h}\right|=1 \mathrm{~V}$ and $\mu C_{O X} W / L=200 \mu \mathrm{~A} / \mathrm{V}^{2}$.
(a) Assuming the input is fed with a sine-wave signal with a 5 V amplitude (i.e., $V_{i n}=5 \sin (\omega t)$ ) and $R_{L} \rightarrow \infty$, sketch the output voltage waveform.
(b) (Continuing from part (a)) For what value of load resistor $R_{L}$ is the peak output voltage reduced to half of the input signal amplitude (i.e., $\left|V_{\text {out }, \text { peak }}\right|=2.5 \mathrm{~V}$ )?
(c) The class B output stage is connected with an op-amp into a feedback configuration as shown in Figure 2(b). The op-amp has an open loop voltage gain $A_{0}=100 \mathrm{~V} / \mathrm{V}$. Sketch the transfer characteristic $v_{\text {out }}$ vs. $v_{i n}$. Assume $R_{L} \rightarrow \infty$.
(d) (Continuing from part (c)) The 5 V -amplitude input signal is now connected to the input of the circuit in Figure 2(b). Assuming the op-amp has a slew rate of $10 \mathrm{~V} / \mu \mathrm{S}$, calculate the maximum allowable frequency of the input signal for the output waveform NOT having distortion due to slew rate limitation.


Figure 2

## PROBLEM 3 (10pts):

The ac schematic of a feedback amplifier is shown in Figure 3 ("ac schematic" means that biasing is not shown, but that you should assume that all devices are biased appropriately.) All transistors have $I_{D}=1 \mathrm{~mA}, W / L=100, k^{\prime}=60 \mu \mathrm{~A} / \mathrm{V}^{2}$, and $\lambda=1 /(50 \mathrm{~V})$.
(a) Determine the type of feedback.
(b) Calculate the loop return ratio, the overall gain $v_{o} / i_{i}$, as well as the input impedance, and the output impedance at low frequencies (i.e. neglect transistor capacitances).
(c) If the circuit is fed from a source resistance of $1 \mathrm{k} \Omega$ in parallel with $i$, what is the new output resistance of the circuit?


Figure 3

## EXTRA PROBLEM FOR EE 240A STUDENTS:

PROBLEM 4 (20pts):
An all-npn Darlington output stage is shown in Figure 4. For all devices $\mathrm{V}_{\mathrm{BE}(\mathrm{on})}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}(\mathrm{sat})}=$ $0.2 \mathrm{~V}, \beta_{\mathrm{F}}=100$. The magnitude of the collector current in $\mathrm{Q}_{3}$ is 2 mA .
(a) If $R_{L}=8 \Omega$, calculate the maximum positive and negative limits of Vo.
(b) Calculate the power dissipated in the circuit for $\mathrm{Vo}=0 \mathrm{~V}$.
(c) Calculate the maximum average power that can be delivered to $R_{L}=8 \Omega$ before clipping occurs and the corresponding efficiency of the complete circuit. Also calculate the maximum instantaneous power dissipated in each output transistor. Assume that feedback is used around the circuit so that Vo is approximately sinusoidal.


Figure 4

