Homework 5

Due: Friday, 28 February 2014 at 1pm

This is an individual assignment!

PROBLEM 1 (10pts):

Fig. 1(A) shows a common source amplifier that is biased using a current mirror. Assume that R_B and C_B have very large values, and that the transistors have the following parameters: L = 120nm, V_{th0} = 0.5V, $k_n' = 200\ \mu A/V^2$, $\gamma = 0$.
Given V_{DD} = 1.5 V, W_1 = 1.92 µm, I_{REF} = 100 µA, and R_L = 1 kΩ:
(a) Assuming $\lambda = 0$, size M_2 (i.e. find W_2) so that the amplifier has a mid-band, small-signal voltage gain $v_o/v_i = 5$. What is the bias current I_{D2} in this case?
(b) Keep the same size for M2 that you found in part (a), but now let $\lambda = 0.4\ V^{-1}$. What is the new bias current I_{D2}? What is the new small-signal voltage gain? Explain the source of mismatch with your results from part (a).
(c) In order to more accurately control the bias current, we could add a cascode device to the amplifier, as shown in Fig. 1(B). Find the bias voltage V_B that will make the bias current I_{D2} match what was found in part (a) exactly. Assume $(W/L)_3 = (W/L)_2$, and $\lambda = 0.4\ V^{-1}$ still.

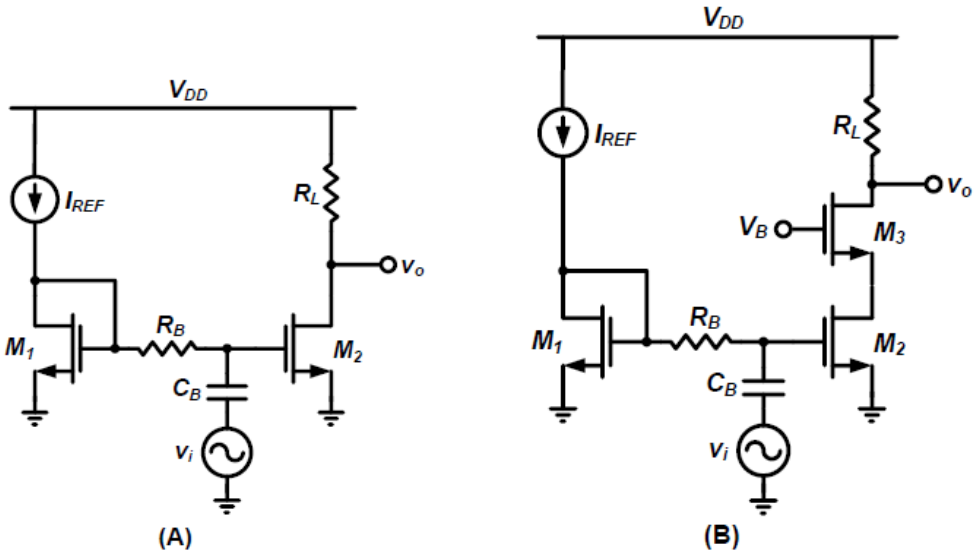

Figure 1

PROBLEM 2 (10pts):

Determine the output resistance of the current mirror in Figure 2 as a function of transistor parameters. Neglect the body-effect. Assume that the amplifier in Figure 2 has finite gain A=100 and infinite input resistance. For small-signal analysis assume $v_o = A(v_+ - v_-)$. Since gain A is high, for DC analysis assume that $v_+ = v_-$. If the size of transistors $M_{1\text{-}4}$ is W/L, find the size of M_5 that minimizes the systematic gain error. What is the resulting gain error?

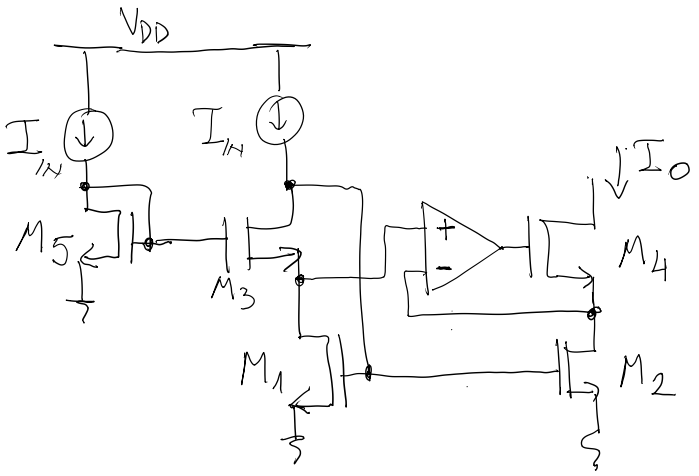

Figure 2

PROBLEM 3 (10pts):

Figure 3 depicts a self-biasing V_t reference circuit which is capable of providing a current reference independent of biasing voltage.

(a) Provide expressions for the DC output current I_{OUT} and biasing currents I_{BIAS1} and I_{BIAS2} in terms of circuit elements and transistor parameters and calculate numerical values. Ignore body effect and channel length modulation.

(b) Calculate the ratio of small-signal variations in I_{OUT} to small-signal variations in V_{DD} at low frequencies. Ignore the body effect but include finite transistor r_o in this calculation.
MOS parameters: $|V_{th}|$=0.5V, k_n'=200μA/V^2, k_p'=100μA/V^2, λ=0.05V^{-1}, V_{DD}=3V, R=1.75kΩ, $(W/L)_1$=12.5μm/0.25μm, $(W/L)_2$=6.25μm/0.25μm, $(W/L)_3$=31.25μm/0.25μm, $(W/L)_4$=6.25μm/0.25μm, $(W/L)_5$=12.5μm/0.25μm, $(W/L)_6$=15.5μm/0.25μm.

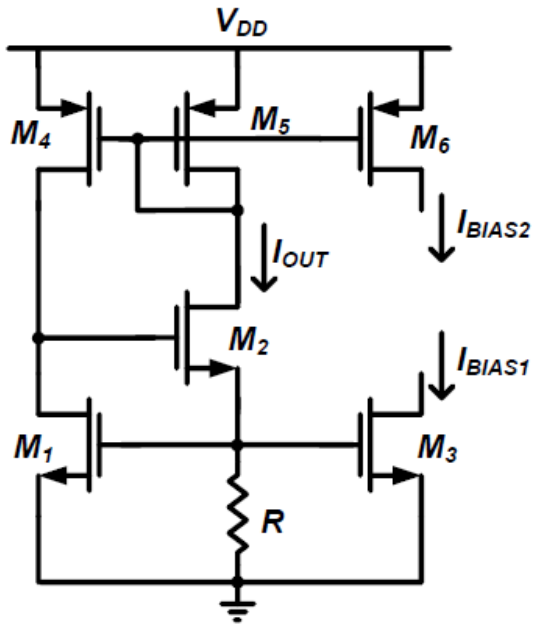

Figure 3

EXTRA PROBLEMS FOR EE 240A STUDENTS:

PROBLEM 4 (10pts):

A band-gap reference circuit is shown in Fig. 4. Assume that $\beta_F \rightarrow \infty$, VA $\rightarrow \infty$, $I_{S1} = 1 \times 10^{-15}$A, and $I_{S2} = 8 \times 10^{-15}$A. Assume the op-amp is ideal except for a possibly nonzero offset voltage V_{OS}, which is modeled by a voltage source in Fig. 4.

(a) Suppose that R_2 is trimmed to set V_{OUT} equal to the target voltage for which $dV_{OUT}/dT = 0$ at T = 25°C when $V_{OS} = 0$. Find dV_{OUT}/dT at T = 25°C when V_{OS} = 30 mV.

(b) Under the conditions in part (a), is dV_{OUT}/dT positive or negative? Explain.

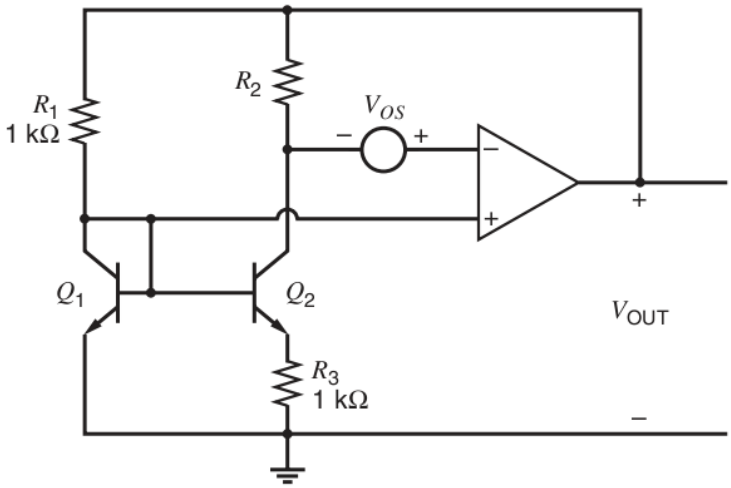

Figure 4

PROBLEM 5 (10pts):

For the bias circuit shown in Figure 5:

a) Determine the bias current. Assume $|V_{th}|$=0.5 V, $k_n' = 200\ \mu A/V^2$, $k_p' = 200\ \mu A/V^2$. Neglect base currents and the body effect.

b) Derive the expression for the temperature dependence of the bias current.

c) Derive the expression for the supply sensitivity of the bias current. Assume $\lambda = 0.05\ V^{-1}$.

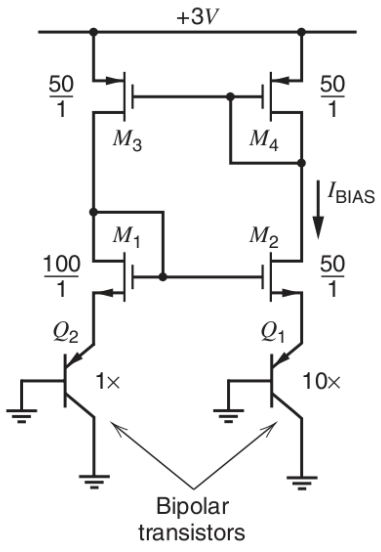

Figure 5