Homework 8

Due: Friday, April 4, 2014 at 1pm

This is an individual assignment!

PROBLEM 1 (15pts):

Consider a two-pole op amp with open-loop transfer function $a(s) = a_0/[(1-s/p_1)(1-s/p_2)]$. Assume that $20\log_{10}(a_0) = 60$dB, and $|p_1|$ is the dominant pole located at $2\pi\times100$kHz.

a. Find the value of p_2 so that the op amp would have a 45° phase margin in unity-gain feedback. Sketch the magnitude and phase Bode plots of the op amp's open-loop transfer function.

b. Let $|p_2|=2\pi\times10$MHz for this and all remaining parts of this problem. Find the op amp's unity-gain frequency and unity-gain phase margin. Sketch the magnitude and phase Bode plots of the op amp's open-loop transfer function.

c. Given what you found in part (b), is it safe to put this op amp into unity-gain feedback? Explain why or why not.

d. We would like to compensate the op amp by using a zero to cancel p_2, so that its open-loop transfer function is now $a(s) = a_0(1-s/z_1)/[(1-s/p_1)(1-s/p_2)]$, with $z_1 = p_2$. What is the compensated op amp's unity-gain frequency and unity-gain phase margin?

e. Realistically, we are unable to match z_1 and p_2 exactly. Repeat part (d) for $z_1 = 2\times p_2$ and $z_1 = 0.5\times p_2$.

PROBLEM 2 (15pts):

Consider an op-amp whose open-loop transfer function is shown in Figure 1a. Assume that the op-amp circuit includes a stage such as that of Figure 1b with *Cx* = 100pF, *Cy* = 5pF, and *gm* = 40mA/V, that the pole at *fP1* is caused by the input circuit of that stage, and that the pole at *fP2* is introduced by the circuit output. Find the value of the compensating capacitor such that the closed-loop amplifier with resistive feedback is stable for any gain (i.e., for *f* – feedback factor up to unity) if the compensating capacitor is connected:

(a) Between the input node *X* and ground,

(b) Between *X* and *Y*, in the feedback path of the transistor.

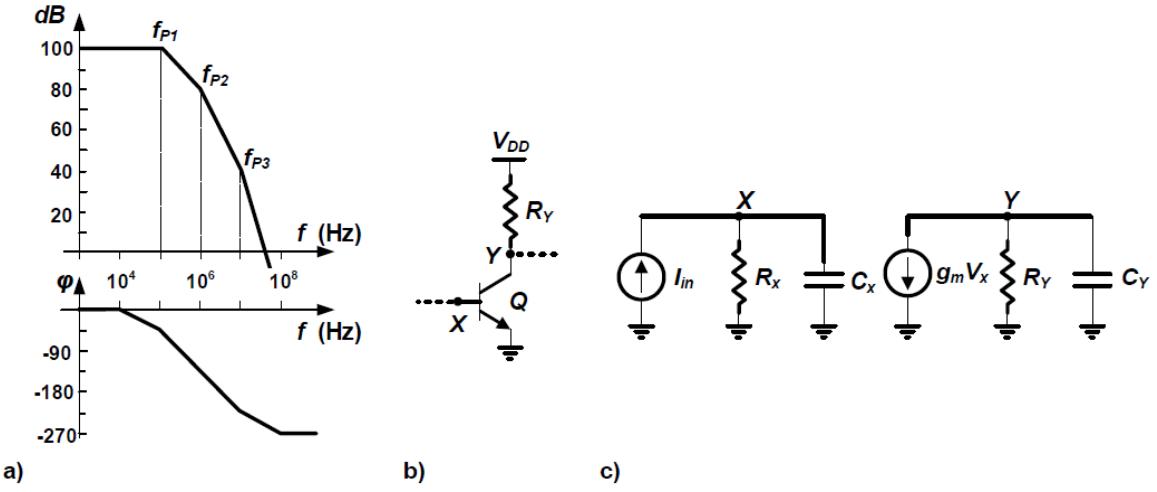

Figure 1

PROBLEM 3 (20pts):

In the amplifier shown in Figure 2 transistors M3-M8 are biased with V_{ov}=200mV. Gates of M3 and M4 are biased to allow maximum undistorted sinusoidal signal at the output.
Calculate all currents, channel widths and the value of capacitor C_c so that the amplifier has DC gain of 20, phase margin of 60 degrees for unity gain feedback, and the unity gain frequency of 50MHz. All transistors have the same channel length. Neglect all parasitic capacitances in this problem.
V_{dd} = 3V, R_L = 10kΩ, C_L = 5pF, $V_{th0,n}$ = 0.5V, k_n' = 250µA/V^2, L=0.5µm, λ=0, γ=0, L_d=0

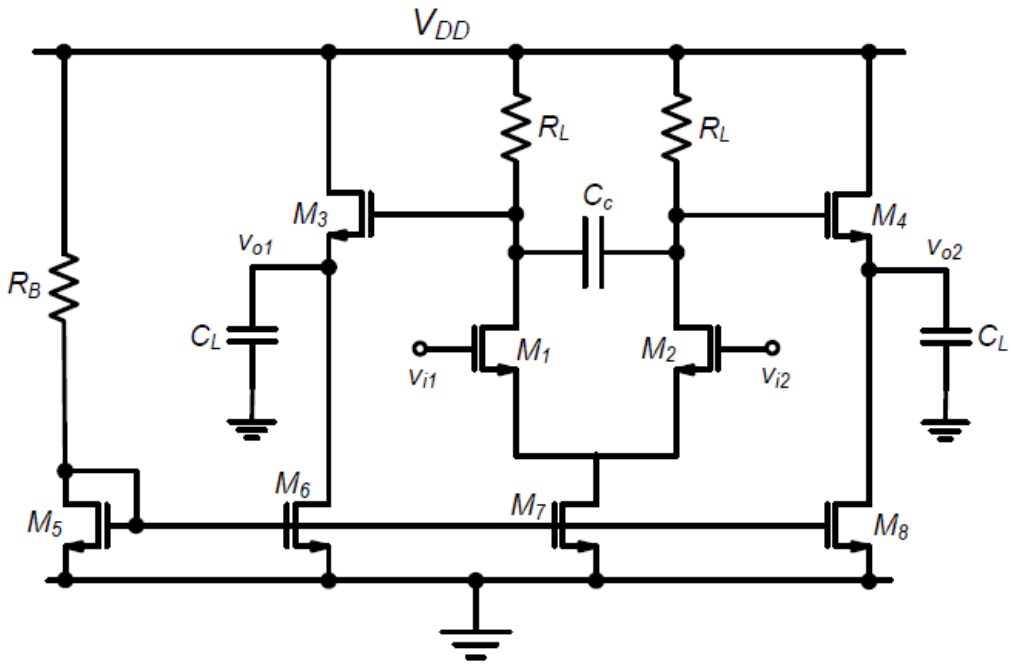

Figure 2

EXTRA PROBLEM FOR EE 240A STUDENTS:
PROBLEM 4 (20pts):
A two-stage op amp has a compensation capacitor connected between the input and the output of its second stage. Assume that the frequency of its second-pole is 60MHz and that this frequency stays constant with changes in the compensation capacitor. Assume the input stage generates a transconductance of 0.70mA/V, and the second stage provides a voltage gain of 100. With the feedback configuration shown in Figure 3, determine the maximum amplitude of the circuit's closed-loop gain due to frequency peaking for the following compensation capacitances:

(a) 0.25pF

(b) 0.50pF

(c) 0.60pF

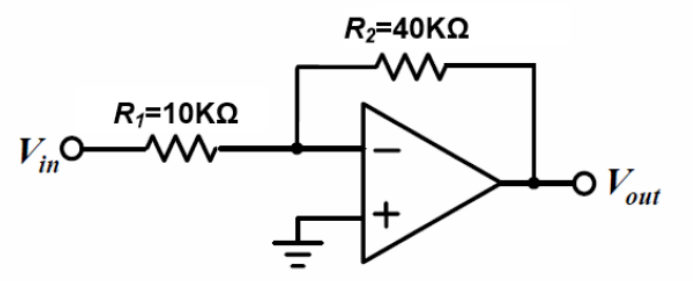

Figure 3