Homework 9

Due: Friday, April 11, 2014 at 1pm

This is an individual assignment!

PROBLEM 1 (20pts):

Figure 1 depicts a simple amplifier circuit using active load. Assume that the output voltage is set at 1V.

(a) Calculate the DC operating points including the current flowing through each branch and DC voltage at each node.

(b) Calculate transistor small-signal parameters (i.e. g_m, g_{mb}, r_o, C_{gs}, C_{gd}).

(c) Provide expressions and calculate the numerical values for the output resistance, R_{out}; and gain, v_{out}/v_{in}.

(d) Estimate the high-frequency cut-off f_H of the amplifier. MOS parameters: (for both NMOS and PMOS, unless otherwise stated)
$|V_{th}|=0.5V$, $k_n'=200\mu A/V^2$, $k_p'=100\mu A/V^2$, $V_{DD}=2.5V$, $\lambda=0.05V\text{-}1$, $\chi=0.1$, $C_{ox}=5fF/\mu m2$, $C_{ol}=3fF$, $C_{sb}=C_{db}=5fF$
$(W/L)_1=2.25\mu m/0.25\mu m$, $(W/L)_2=4.5\mu m/0.25\mu m$, $(W/L)_{3,4}=3.75\mu m/0.25\mu m$,
$(W/L)_{5,6}=11.25\mu m/0.25\mu m$, $(W/L)_7=37.5\mu m/0.25\mu m$, $(W/L)_8=7.5\mu m/0.25\mu m$,
$(W/L)_9=6.25\mu m/0.25\mu m$, $(W/L)_{10}=12.5\mu m/0.25\mu m$, $(W/L)_{11}=11.25\mu m/0.25\mu m$.
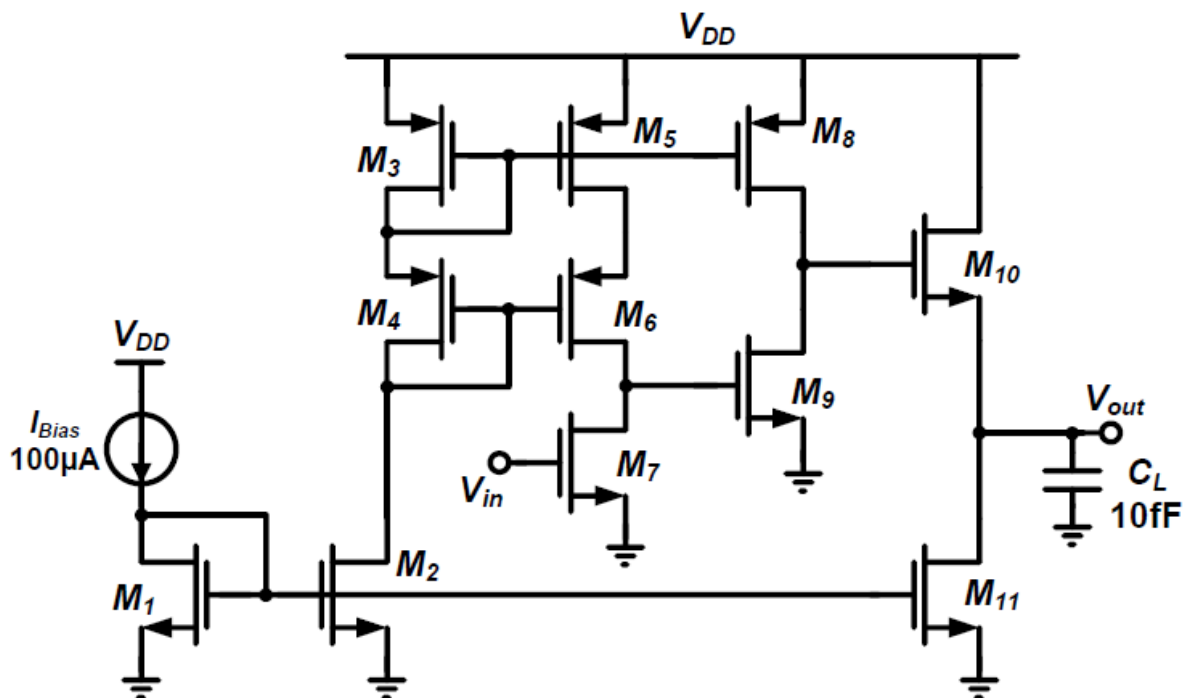

Figure 1

PROBLEM 2 (20pts):

For the two-stage amplifier shown in Figure 2, assume $I_{Bias} = 20\mu A$, and the output voltage V_{out} is biased to 0V. Determine the size of MOS transistors and then compensate the amplifier to satisfy the following specifications:

i) Low-frequency open-loop gain $\geq$ 90dB

ii) Unity-gain bandwidth $\geq$ 3MHz

iii) Phase margin $\geq 60°$ for unity-gain feedback

iv) Slew rate $\geq 4V/\mu s$

v) Peak-to-peak output swing $\geq$ 9.5V
You should size *M9* to move the zero introduced by the pole splitting to infinity.
MOS parameters:
$|V_{th}| = 0.7V$, $\mu_n = 700cm^2/V$-s, $\mu_p = 350cm^2/V$-s, $\lambda_n = 0.015V^{-1}$, $\lambda_p = 0.03V^{-1}$, $L_{min} = 1\mu m$, $C_{ox} = 86.3nF/cm^2$, $C_{ol} = 0.35fF/\mu m$, $C_{j0} = 0.15fF/\mu m^2$, $C_{jsw0} = 1fF/\mu m$, $m_j = 0.5$, $m_{jsw} = 0.5$, $\varphi 0 = 0.65V$.
Note: All of transistor dimensions should be larger than L_{min}. Use the λ design rule described in Lab 3 write-up to determine the MOS parasitic capacitors, if needed.
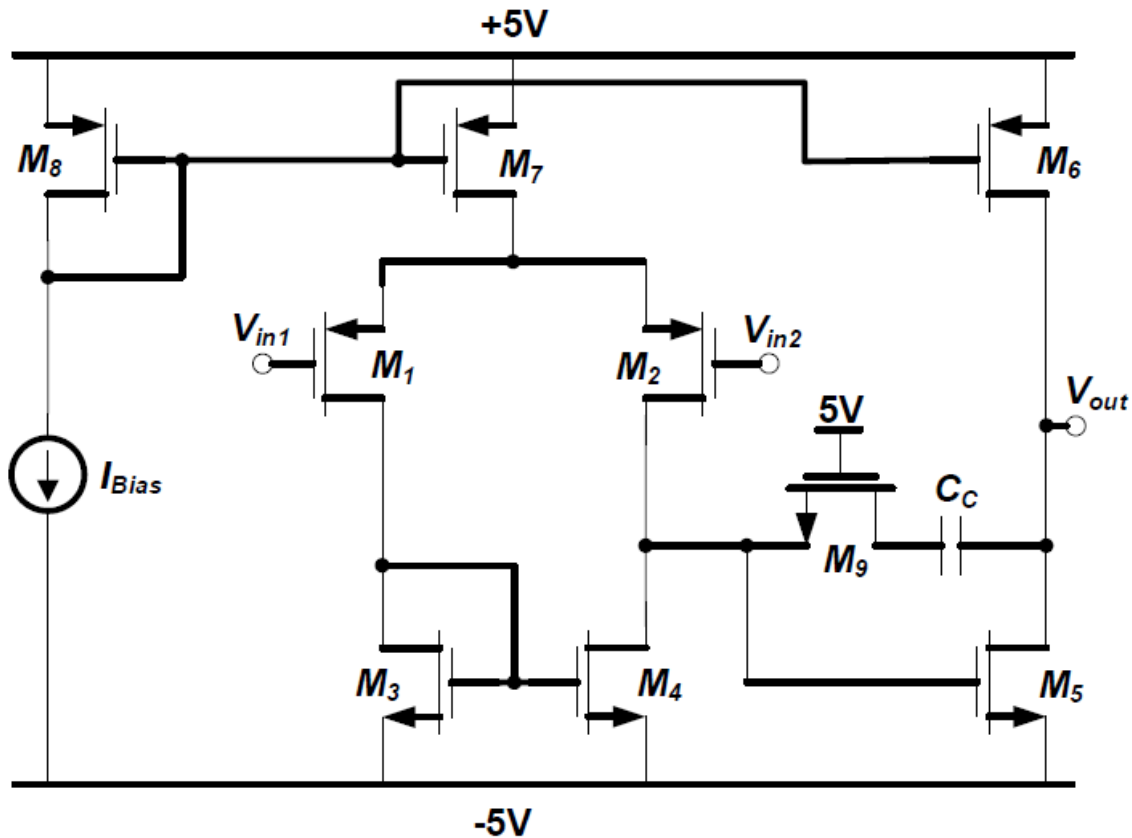

Figure 2

PROBLEM 3 (20pts):

In this problem, you will simulate using Hspice the op amp given in "ee140_hw9.sp" below. Its accompanying device model is given in "ee140_hw9_model.sp" below. For your convenience, the op amp circuit is pictorially shown below in Figure 3. Please give all gain values and ratios in dB.
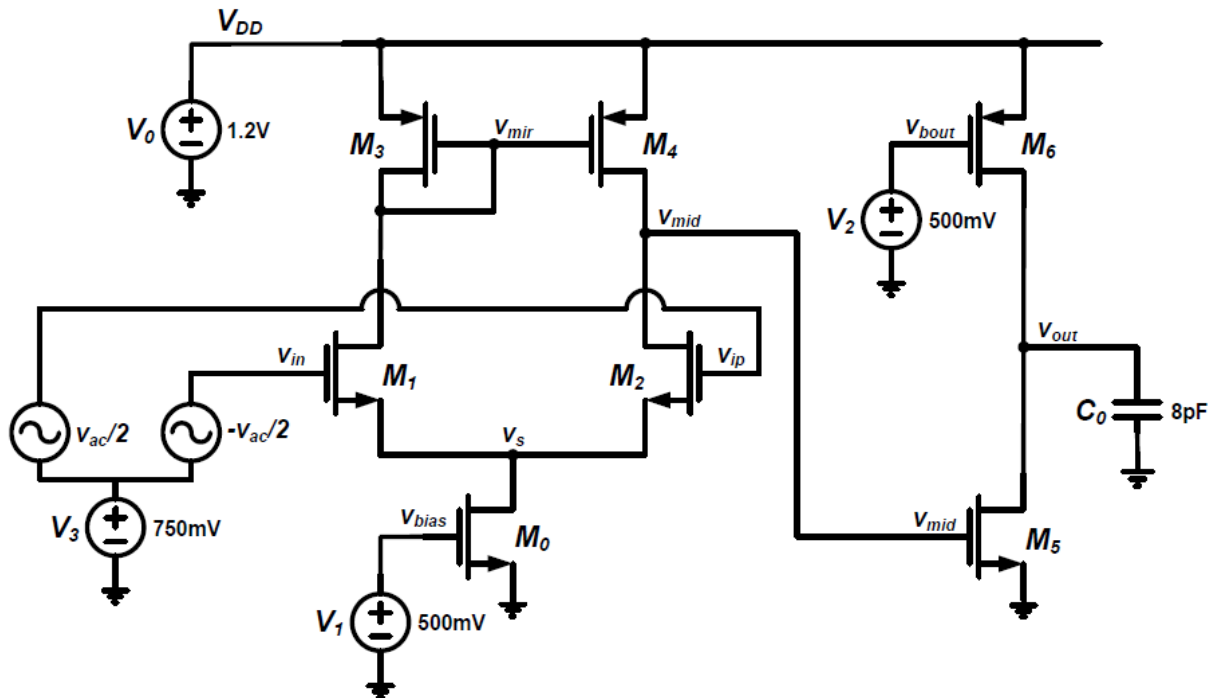

Figure 3

a. Simulate the open loop AC gain and phase of the op amp. What is the op amp's gain at low frequencies? What is the op amp's unity gain frequency? What is the op amp's unity gain phase margin?

b. Simulate the common mode gain of the op amp by applying positive *vac* to both inputs. What is the op amp's common mode gain at low frequencies? What is the op amp's CMRR?

c. Simulate the power supply gain of the op amp:
    i. Turn off the AC signal at the op amp's inputs.
    ii. Add an AC signal to the power supply voltage source *V0*.
    What is the op amp's power supply gain at low frequencies? What is the op amp's PSRR?

d. Simulate the output swing of the op amp using DC sweep analysis:
    i. Sweep the DC voltage at one of the op amp's inputs around its bias point.
    ii. Take the derivative of the op amp's DC output voltage with respect to the swept input. Make sure there is enough resolution in your sweep to get an accurate result.

For the purpose of this course (and your project), we will define the op amp's output swing range as the DC output voltages at which *dVout/dVin* becomes 1/10 the nominal differential gain (from part (a)). What is the op amp's output swing range?

e. Simulate the common mode input range of the op amp using DC sweep analysis:
 i. Put the op amp into unity gain feedback.
 ii. Sweep the DC voltage of the op amp's input from 0 to VDD.
 iii. Take the derivative of the op amp's DC output voltage with respect to the swept input.

For the purpose of this course (and your project), we will define the op amp's input range as the DC input voltages at which *dVout/dVin* becomes 1/2 in unity gain feedback. What is the op amp's common mode input range?

Model and netlist files:

Use the text below to create the op-amp netlist file "ee140_hw9.sp".

```
* EE140 HW#9 Problem 3

.lib 'ee140_hw9_model.sp' tt

.param len = 100n
.param wtail = 10u
.param wn = 5u
.param wp = 10u
.param vb1 = 500m
.param vb2 = 750m
.param vb3 = 500m
.param CL = 8p

v0 vdd   gnd 1.2
v1 vbias gnd vb1
v2 vbout gnd vb3

v3 vdc gnd vb2
v4 vac gnd AC=1
e0 vip vdc vcvs vac gnd 0.5
e1 vin vdc vcvs vac gnd -0.5

m0 vs    vbias gnd gnd nmos L=len W=wtail
m1 vmir vin    vs  gnd nmos L=len W=wn
m2 vmid vip    vs  gnd nmos L=len W=wn
m3 vmir vmir  vdd vdd pmos L=len W=wp
m4 vmid vmir  vdd vdd pmos L=len W=wp

m5 vout vmid  gnd gnd nmos L=len W=wn
m6 vout vbout vdd vdd pmos L=len W=wp

c0 vout gnd CL

.op
.option post = 2 nomod

.end
```

Use the text below to create the op-amp netlist file "ee140_hw9_model.sp".

```
.LIB TT
.lib 'ee140_hw9_model.sp' ee140_hw9_model
.ENDL TT

.LIB ee140_hw9_model

.model nmos nmos(

+Level = 1
+VTO = 0.3
+KP = 200u
+GAMMA = 0.2
+LAMBDA = 0.2
+TOX = 2.2n
+PHI = 0.6

)

.model pmos pmos(

+Level = 1
+VTO = -0.3
+KP = 100u
+GAMMA = 0.2
+LAMBDA = 0.2
+TOX = 2.2n
+PHI = 0.6

)

.ENDL ee140_hw9_model
```