CMOS - op-amp applications.

a) External amplifiers (feedback is set by external components)

\[ \frac{V_o}{V_i} = -\frac{R_S}{R_f} \quad \text{as long as} \quad A \quad \text{large} \]

b) Internal amplifiers

\[ \frac{\Delta V_o}{\Delta V_i} = \frac{28}{25} = -\frac{C_S}{C_f} \]

Switch-cap amplifiers:

\[ \phi_1, \phi_2 \]

No DC-bias
\( \Phi_1 \text{ high: (input sample phase)} \)

\[ Q_1 = (V - V_i) \cdot C_s + 0 \cdot C_f = -V_i \cdot C_s \]

\( \Phi_2 \text{ high: (transfer phase)} \)

\[ Q_2 = (V_s - 0) \cdot C_s + (V_s - V_o) \cdot C_f = -V_o \cdot C_f \]

Charge conservation: \( Q_1 = Q_2 \)

\[ -V_i \cdot C_s = -V_o \cdot C_f \]

\[ \Rightarrow \quad \frac{V_o}{V_i} = \frac{C_s}{C_f} \]
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\[ Q_1 = -V_i C_s \]

\[ Q_2 = \left( -\frac{V_0}{a} - \delta \right) \cdot C_s + \left( -\frac{V_0}{a} - V_0 \right) \cdot C_f + \left( -\frac{V_0}{a} \right) C_p \]

\[ Q_1 = Q_2 \Rightarrow \frac{V_0}{V_i} = \left( \frac{C_s}{C_f} \right) \cdot \frac{1}{1 + \frac{1}{a} \left( \frac{C_s + C_f + C_p}{C_f} \right) \left( a - 1 \right)} \]

\[ \xi = \frac{1}{1 + a \cdot \frac{C_f}{C_s + C_f + C_p}} \]

Limitations:
- Matching \( C_s \) & \( C_f \)
- Need large open-loop gain \( a \)
- Offset \( \neq 0 \)
- Switches leak
- Charge injection & clock feed through

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Basic two-stage CMOS op-amp:

1. Gain: \( \frac{V_o}{V_{in}} = \frac{V_o}{V_{1}-V_{in}} = g_{m1,2}(V_{o2}||V_{o4}) \cdot g_{m5} \cdot \frac{V_{o6}||V_{o5}}{V_{ss}} \)

Want gain to be big: \( I_{bias} \downarrow, L \uparrow \)

\( \Rightarrow \) trade-off gain vs. speed

2. \( R_{in} = \infty \)

3. \( R_{out} = V_{o5}||V_{o6} < o.o. \) via driving our output caps
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4) Output swing:

\[ V_{o_{\text{max}}} = V_{DD} - 1V_{ou1} \]

\[ V_{o_{\text{min}}} = V_{SS} + V_{ou6} \]

5) Input swing: CMR: \[ \frac{V_{IC}}{V_{IC}} \]

\[ V_{DD} \]

i) \( V_{IC} \downarrow \)

\[ V_{IC_{\text{min}}} = V_{SS} + V_{ou7} + V_{th1} \]

\[ M_7 \text{ in } \text{SAT} \]

ii) \( V_{IC} \uparrow \), \( M_7 \text{ in SAT} \)

\[ \left( V_{G3} - \right) \frac{V_{th3}}{V_{G3}} \]

\[ V_{IC_{\text{max}}} = V_{DD} - \left| V_{th3} \right| - \left| V_{ou3} \right| + V_{th1} \]

\[ V_{th1} > V_{th3} \]
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6. Offset:
   a) Systematic offset:

\[ V_{os1} \]
\[ A_1 \]
\[ V_{os1} \]
\[ A_2 \]
\[ V_{os2} \]
\[ V_o \]

Design for \( V_{os1} = 0 \) (systematic) and minimize \( V_{os1} \) (random)

Single scenario:

\[ V_{os1} = 0 \]
\[ V_{os4} \]
\[ V_{os5} \]
\[ k = \frac{1}{2} \]

\[ \frac{W}{L} \]
\[ \frac{W}{2} \]
\[ \frac{W}{2} \]

\[ V_{ou3} = V_{ou4} = V_{ou5} \]

\[ k > \frac{1}{2} \]

\[ \frac{W}{2} \]
\[ 2k \left( \frac{W}{L} \right)^{\frac{5}{3}} \]

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