Homework-4 Solutions and Grading rubric

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Q-1 16spMidterm1C problem-6 (http://inst.eecs.berkeley.edu/~ee140/sp18/exams/16spMid1C.docx)
The four transistors shown below are all biased at a current of 1uA. The NMOS device M1 is in sub-threshold, with $V_{GS}-V_{T}=-200\text{mV}$, and $n=1.5$. The NMOS device M2 is velocity saturated with $V_{GS}-V_{T}=100\text{mV}$. The NMOS device M3 is in saturation, with a channel field of approximately $0.1\text{V/um}$ and $V_{GS}-V_{T}=100\text{mV}$.

A) Approximately what change in $V_{BE}$ will cause the collector current to increase by a factor of 10?

B) Approximately what change in $V_{GS1}$ will cause the drain current in M1 to increase by a factor of 10?

C) Approximately what change in $V_{GS2}$ will cause the drain current in M2 to increase by a factor of 10?

D) Approximately what change in $V_{GS3}$ will cause the drain current in M3 to increase by a factor of 10?

** Really, $V_{ov}$ goes up by $rt(10)x$ to $0.32\text{V}$, so $V_{GS}$ only needs to go up by 220mV (200mV was fine if you showed that you got there by approximating $rt(10)~3$).

\[ \Delta V_{BE} = 60\text{mV} \quad \Delta V_{GS1} = 1.5 \times 60\text{mV} = 90\text{mV} \quad \Delta V_{GS2} = 1\text{V} \quad \Delta V_{GS3} = 0.32\text{V} \]

\[ \begin{align*}
\text{(A)} & \quad V_{BE1} = VT \ln \left( \frac{I_{D}}{I_{S}} \right) \\
\text{(B)} & \quad V_{BE2} = VT \ln \left( \frac{I_{D2}}{I_{S}} \right) \\
\text{(C)} & \quad V_{BE} = VT \ln \left( 10 \right) = 0.59786\text{mV} \\
\text{(D)} & \quad V_{ov} = V_{GS} - V_{TH} = \sqrt{2I_{D}/B} = \frac{1}{B}I_{D}
\end{align*} \]

\[ \begin{align*}
\text{(A)} & \quad \text{velocity} \\
\text{(B)} & \quad \text{in a saturation region} \\
\text{(C)} & \quad \text{for 10x} \ \text{Io} \ \text{Vov increases by 10x} \\
\text{(D)} & \quad \text{for 10x} \ \text{Io} \ \text{increase,} \\
\text{(E)} & \quad V_{ov} \text{ goes up by } \sqrt{I_{D}} = 3.16 \\
\text{(F)} & \quad V_{ov} = 3.16 \times 0.1\text{V} = 0.316\text{V}
\end{align*} \]

Total: 8 pts
For each (a-d) 2pts
+1 pts for correct eqn.
+1 for correct calc. value.
Q-2) First we assume, $V_{TH,n} = |V_{TH,p}| = 0.5V$. While we replace NMOS with PMOS and PMOS with NMOS the goal is to keep the same drain/source potential. The orientation of drain/source is determined by the voltage magnitude as MOS device is symmetric about drain – source. However, the new gate voltage is calculated so that gate-source voltage is same, before and after the devices are swapped.

<table>
<thead>
<tr>
<th>OFF</th>
<th>Lin</th>
<th>Sat</th>
<th>Linear</th>
<th>Sat</th>
<th>Sat</th>
<th>Off</th>
<th>Sat</th>
</tr>
</thead>
<tbody>
<tr>
<td>New $V_{gate}$</td>
<td>3.0V</td>
<td>3.0V</td>
<td>-1.0V</td>
<td>1.0V</td>
<td>3.0V</td>
<td>3.0V</td>
<td>-1.0V</td>
</tr>
<tr>
<td>V$_{dsat}$ (if Sat)</td>
<td>0.5</td>
<td>1.5V</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Total: 12 pts
If device in Sat: +1 pt of region of operation
+1 pt of right V$_{dsat}$ value
For the rest: +1 pt of region of operation
Q-3)

0.5 μm process $C_{ox} = 5fF/\mu m^2$ 
$C_{ox} = 200fA/V^2$ $\mu p_{ox} = 100\mu A/V^2$

$\lambda = \frac{1}{10}$, $L = 0.5\mu m$, $V_{th, n} = -V_{th, p} = 0.5V$
$A_{v} = 200$

$v_{dd} = 2.5V$

$V_{pp} = 4mV$

$V_{in} = 1.0\mu A$

$V_{out} = 1.0\mu A$

$g_{m}/L = V_{GB} \geq 1.0 \text{ grad/sec}$
$\Rightarrow g_{m} = 1.0 \text{ ms}$

Our aim is to minimize $I_{D}$ for lowering power.

Thus, to achieve this we pick $V_{ov}$ as small as possible.

$V_{pp} = 0.1 + 0.5 = 0.6V$. Output swing required = 0.3V to 2.2V. Thus,
$V_{ov}$ of NMOS atleast is 0.3V and
$V_{ov}$ of PMOS = 0.3V

PMOS sizing $I_{D} = 30\mu A$ $V_{ov}$ of PMOS = 0.3V → (Pick)

$V_{bg,p} = 0.8V$ $\Rightarrow V_{sat,p} = 1.7V$

Pick $L_{p} = L_{n} = 10\mu m \Rightarrow I_{D} = \frac{1}{2} \left( \frac{W}{L} \right) \mu p_{ox} (V_{pp})^{2}$

$W_{p} = 11.1\mu m$
Step-3  Calculate "L"

\[ Av = -g_{m} R_{VT} \]

\[ R_{VT} = \frac{\gamma_{n}}{\gamma_{p}} = \frac{1}{2 \lambda I_{D}} \]

\[ I_{D} = \frac{-1}{2 \lambda I_{D}} \times \frac{2 I_{D}}{V_{OV}} = -\frac{1}{\lambda V_{OV}} \]

\[ \lambda V_{OV} \]

\[ \frac{1}{\lambda} = \frac{V_{A} \times \frac{L}{L_{min}}}{} \]

\[ L_{min} \]

\[ L = \frac{10V}{100} = 10 \mu m \]

\[ L = 10 \mu m \]

This is less than \( Av = 200 \) required by design.
To achieve required gain \( L = 2L_{min} \) would be sufficient.

\[ \therefore \ L = 10 \mu m \]

Step-4  Calculate "W"

\[ g_{m} = \left( \frac{L W}{L} \right) \mu \text{mcm} \left( V_{OV} \right) = W \mu \text{mcm} \left( \frac{V_{OV}}{L} \right) \]

constant for a fixed required Av

\[ \therefore \ W = 50 \mu m \]

Step-5  Calculate "C_{IN}"

\[ C_{IN} = (g_{s} + (1 - Av) C_{gd}) \]

\[ C_{gd} = W C_{al} = 50 \times 0.5 = 25 \text{pF} \]
Value of $C_{IN}$ found in the previous calculation is just too large. Assume that we intend to minimize it. To do so the $V_{ov}$ should be increased from 0.1V to the 0.3V. Note that the output swing requirement would allow $V_{ov}$ to be increased only till 0.3V.

Given $C_{IN}$ is large, we would like to minimize it.

First, let's see if "W" can be reduced.

$$g_m = \left(\frac{W}{L}\right) \rho \mu C_{ov} V_{ov} \Rightarrow \frac{V_{ov}}{L} \text{ is constant}$$

If $V_{ov}$ fixed, $g_m \Rightarrow \text{"W" is fixed.}$

Thus, $W/L$ is fixed $\Rightarrow$ $C_{gd}$ is fixed and overlap cap fraction of $C_{gs}$ is also fixed.

What about $(2/3) W \cdot L \cdot C_{ox}$? $\Rightarrow$ if $V_{ov} = 0.3$ then $L \rightarrow 3L$

To keep same gain $A_V$.

Thus $C_{gs}$ would rather increase.

Hence, $C_{IN}$ is minimum for $V_{ov} = 0.1V$ while $R_{on}$ is also lowest.

Total pts: 9 pts
+2 pt: Identify that to reduce $C_{IN}$ we need to look for lowering “W” and “L”
+2 pt: Establish that $V_{ov}/L$ is constant
+1: Prove that “W” stays constant
+1: Thus, $C_{gd}$ stays constant
+2: Show that choosing $V_{ov} = 0.3$ will instead increase $C_{gs}$
+1: $C_{IN}$ is minimum with $V_{ov} = 0.1$. Can’t be reduced further.
Q-5)

a, b, c, d)

Total Pts: 13pts

a) 3pt: +1 for right ID equ. +1 for each ID value.
b) 3pt: +1 for right Vgs equ. +1 for each Vov value.
c) 2pt: +1 for right eqn for ro and gm
d) +2 for right intrinsic gain. If you approx. and derived overall gain, that’s fine too.
e) 3pt: +1 for right gm, ro, Av, wp and wu for each o/p bias values. Note not to double penalize. E.g. Wrong id is -1pt but the resulting error in ro will not receive -1pt as long as it is calculated correctly though with wrong ID value.

The intrinsic gain, Av of NMOS is given by,

\[ Av = \frac{Z}{\lambda \sqrt{2(V_{DD}-V_{OUT})}} \]

As mentioned Av is the intrinsic gain of NMOS. The overall gain = \(-g_m(r_o || R_L || C_L)\) \(-g_m R_L\)
Note that the intrinsic gain, $A_v$, can be re-written as, 

$$A_v = \frac{2V_a \cdot L}{(L_{\min} \cdot V_{ov})},$$

which is quite interesting as it suggests that the intrinsic gain is primarily governed by $V_{ov}$ as $V_a$ is determined by technology.

e)

<table>
<thead>
<tr>
<th>$V_{out}$</th>
<th>$I_D$</th>
<th>$g_m$</th>
<th>$r_o$</th>
<th>$A_{V0}$</th>
<th>$\omega_p$</th>
<th>$\omega_a$</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0V</td>
<td>1mA</td>
<td>20mS</td>
<td>100kΩ</td>
<td>20</td>
<td>10Mrad/s</td>
<td>200Mrad/s</td>
</tr>
<tr>
<td>6.0V</td>
<td>4mA</td>
<td>40mS</td>
<td>25kΩ</td>
<td>40</td>
<td>10Mrad/s</td>
<td>400Mrad/s</td>
</tr>
<tr>
<td>1.0V</td>
<td>9mA</td>
<td>60mS</td>
<td>11.1kΩ</td>
<td>60</td>
<td>10Mrad/s</td>
<td>600Mrad/s</td>
</tr>
</tbody>
</table>

Q-6) Let’s assume that the threshold voltages of PMOS and NMOS devices is also equal. Thus, $V_{TH,n} = V_{TH,p}$.

a) All the device carry the same drain current, $I_D$. By quadratic model: $I_D = \frac{1}{2}(W/L) \mu_n C_{OX} V_{GS,n}^2$. It is given that $(W/L) \mu_n C_{OX} = (W/L) \mu_p C_{OX}$. Under this give condition, the equal $I_D$ through all devices ensures the over-drive is also equal.

b) Under the given conditions, we can write an expression for generic over-drive voltage that applies to both NMOS and PMOS as,

$$V_{ov} = \frac{2I_D}{\mu_n p C_{OX}(W/L)_{n/p}}; V_{GS,n}^{min} = V_{SC,p}^{min} = V_{ov} + V_{TH,n/p}$$

Using this $V_{ov}$ value, the maximum input voltage for $M_1$, $V_{in,max} = V_{DD} - V_{SC,p}^{min}$ while the minimum bias voltage for $M_4$, $V_{BN1,min} = V_{SC,n}^{min}$.

c) Minimum gate voltage of $M_3$ that ensures both $M_3$ and $M_4$ stays in saturation can be found by ensuring $V_{S3,min}$ is atleast equal to the $V_{ov}$ of the $M_4$. Thus

$$V_{BN2,min} = V_{GS,n}^{min} + V_{S3,min} = V_{GS,n}^{min} + V_{ov}$$

Thus, the minimum source of $M_4$ and $M_3$ is equal. However, this ensures that the $M_4$ is just on the verge of saturation. If $V_{BN2,min}$ drops even marginally, then $M_4$ will be pushed into linear region.

d) Similar to (c), the maximum gate voltage of $M_2$ is $V_{in,max} = V_{DD} - V_{SC,p}^{min}$. This ensures that both $M_1$ and $M_2$ stays in saturation.

e) With the minimum gate voltage of $M_3$ as in (c), the node $V_{out}$ can swing as low as $2V_{ov}$ before $M_3$ leaves saturation. Similarly, with the maximum gate of $M_2$ as in (d), the high possible $V_{out}$ swing is $V_{DD} - 2V_{ov}$ before $M_2$ leaves saturation. Thus, the output swing, $V_{out,pp} = V_{DD} - 2V_{ov}$.

f) It is fair to assume that the body-source are connected together for each device. Thus, $V_{BS,n} = V_{BS,p} = 0$. As a result, the $g_{mb,n} = g_{mb,p} = 0$. With this assumption, the “looking-up” ($R_{up}$) and “looking-down” ($R_{down}$) impedance at $V_{out}$ node can be expressed as,

$$R_{up,vout} = g_{m,m2}(r_{o,M1}r_{o,M2}) + r_{o,M1} + r_{o,M2} = r_o (g_m r_o + 2)$$

$$R_{down,vout} = g_{m,m3}(r_{o,M3}r_{o,M4}) + r_{o,M3} + r_{o,M4} = r_o (g_m r_o + 2)$$

The total output impedance is then given by,

$$r_{o,vout} = R_{up,vout} | R_{down,vout} \approx g_m r_o^2 / 2$$

g) The “looking-up” ($R_{up}$) and “looking-down” ($R_{down}$) impedance at source of $M_3$ can be expressed as,
\[ R_{up,M3} = (R_{up,vout} + r_{o,M2})/(1 + g_{M2}r_{o,M2}) = r_o(g_m r_o + 3)/(g_m r_o + 1) \]

\[ R_{down,M3} = r_{o,M4} = r_o \]

The total impedance at the source of M3 is then given by, \( r_{o,M3} = R_{up,M3}||R_{down,M3} = r_o/2 \)

h) Yes, the total impedance seen at the source of M2 and M3 are equal as the same current flows through all devices M1-M4 that has same \((W/L)\mu_nC_{OX} = (W/L)\mu_pC_{OX}\). +1 for right expression

i) Gain of the amplifier, \( A_v = -g_{m,M1}r_{o,vout} = -g_m r_o(g_m r_o + 2)/2 \approx -(g_m r_o)^2 \) +1 for right expression

j) Gain from input to the source of M2: \( A_{v2} = g_{m,M1}r_{o,M2} = g_m(r_o)(g_m r_o + 3)/(g_m r_o + 1) \approx g_m r_o/2 \)

2pts: +1 Cin eqn. +1 Cin value

k) The input capacitance, \( C_{in} = C_{gs} + (1-A_{v2})C_{gd} \) where \( C_{gs} = (2/3)W/LC_{OX} + WC_{ov} \) and \( C_{gd} = WC_{ov} \)

l) Load capacitance is the sum of total parasitic capacitance at the output node, which is given as \( C_o \).

3pts: +1 for each cp,vout, UGB and o/p pole

Unity gain bandwidth = \( g_m,M1/C_o \)

Output pole = 1/\( r_{o,vout}C_{p,vout} = 2/g_m r_o^2 C_o \)

Q-7)
Now let’s assume that we double the overdrive voltage on all the devices. This can be done by 4x increase in the drain current for the same device size or for the same drain current but with 4x lower W/L.

Scenario-1: 4x increase in drain current for the same device size.

<table>
<thead>
<tr>
<th>Swing</th>
<th>Reduces to: ( V_{out,pp} = V_{DD} - 4V_{ov} )</th>
<th>Pole Freq.</th>
<th>Increases by 8x</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>Reduces by 4x: ( r_o ) ↓ by 4x, ( g_m ) ↑ by 2x</td>
<td>Unity-gain freq.</td>
<td>Doubles as ( g_m ) increases by 2x</td>
</tr>
</tbody>
</table>

Scenario-2: 4x smaller size (reduced W/L) for the same drain current.

<table>
<thead>
<tr>
<th>Swing</th>
<th>Reduces to: ( V_{out,pp} = V_{DD} - 4V_{ov} )</th>
<th>Pole Freq.</th>
<th>Unchanged</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>Reduces by 4x: ( g_m ) ↓ by 2x</td>
<td>Unity-gain freq.</td>
<td>Reduces by 2x: ( g_m ) ↓ by 2x</td>
</tr>
</tbody>
</table>

Total: 4 pts
Either of the approach is correct
+1 pts of each swing, \( A_v \), wp and wu.
Grading rubric:
First, please identify whether you belong to EE140/240a.

Rubric for EE140:
Max. points: 86

Q-1) Total points 8
   a) 2 b) 2 c) 2 d) 2

Q-2) Total points: 12
   a) 2 b) 2 c) 1 d) 1 e) 1 f) 1 g) 2 h) 1 i) 1

Q-3) Total points: 16

Q-4) Total points: 9

Q-5) Total points: 13
   a) 3 b) 3 c) 2 d) 2 e) 3

Q-6) Total points: 24
   a) 1 b) 3 c) 2 d) 2 e) 2 f) 3 g) 3 h) 1 i) 1 j) 1 k) 2 l) 3

Q-7) Total points: 4

Rubric for EE240a:
Max. points: 106

Q-8) Total points 20
Calc. using Sub-Vt models: +5
Calc with vel. Sat models: +5
Estimate using Intel 14nm FinFets: +10

Grading guidelines:
1) It important to get the approach right. You should grade a right approach at 60% for grade.
   E.g. 3/5
2) Next, important point is to get right numerical answer. Full grade is reserved for this purpose.
3) Numerical error should cost you 20%
   E.g. 1 numerical error in a 5pt problem is 4/5
4) If approach is correct and problem has multiple numerical error, you at least get 60%
   E.g. 3 numerical error in a 5pt problem is 3/5