EE 140/240A Prof. Pister
Spring 2018

Homework Assignment #6

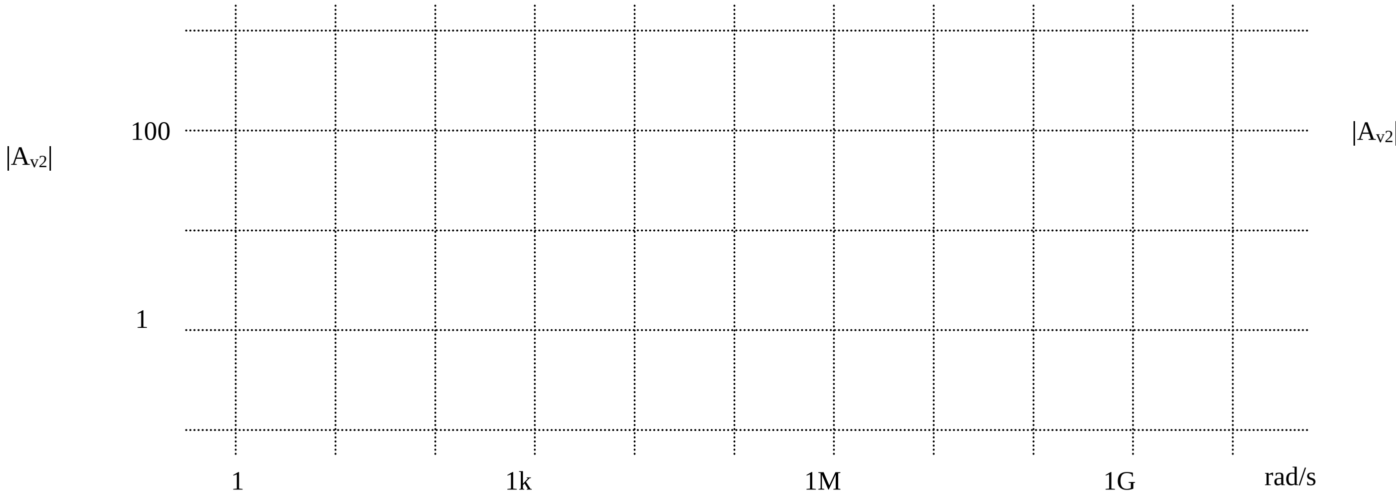
Due by online submission **Wednesday** 3/7/2018 (Thursday 9am)

1. Check out the datasheet for the K2-W tube op-amp. This op-amp, released in 1952, was the first production op-amp. It runs from a +/-300V supply, and has a bandwidth of 300kHz (or k-cycles/s, as they said back then – the unit Hertz not having been established yet). There's a schematic on page 2. Pins 1, 2, and 6 on the bottom of the figure are V+, V-, and Vout. VR1 and VR2 are neon bulbs that provide a low impedance level shift of roughly 100V to center the output between the rails. Redraw, print out, or cut and paste that schematic, and identify (circle and label)
   a. input differential pair
   b. diff-pair load resistor
   c. tail current resistor.
   d. Estimate the common mode gain and write it near the tail resistor.
   e. Common-cathode gain stage (like CS or CE)
   f. Cathode-follower output stage (like source-follower or emitter follower, CD, CC)
   g. Miller-multiplied compensation capacitor from the output back to the input of the gain stage.
   h. Bonus points if you can identify positive feedback in this amplifier, designed to increase the low-frequency gain (which ended up at about 20,000).
2. You have an opamp with a low-frequency gain of 1,000 and a single pole at 100Mrad/s. Plot the location of the pole as a function of the feedback factor f from f=0 to 1. Now with f=0.1
   a. Sketch the Bode plot of the closed-loop amplifier
   b. What is the fractional gain error?
   c. What is the time constant of the step response? How does it compare to the open-loop time constant?
   d. What is the unity gain frequency? How does it compare to the open-loop unity gain frequency?
3. You have an opamp with a low-frequency gain of 1,000 and three poles at 100Mrad/s. Plot the location of the three poles as a function of the feedback factor f. At the point where the poles cross the jw axis, annotate the plot with the value of f that gives this pole location.
4. Estimate the output resistance of a CMOS differential amplifier with current mirror load. You may assume that $g_m r_o >> 1$ for all combinations of g_m and r_o. The following steps may help.
   a. Estimate the impedance seen looking into the source of M1A
   b. Estimate the impedance seen looking down from the source of M1B
   c. Estimate the impedance seen looking into the drain of M1B
   d. For the Ro calculation, estimate i_{d1B} as a function of vo.
   e. The current in i_{d2B} is due to both the output resistance and the mirrored current. Estimate both parts.
   f. Estimate the total output current io = $i_{d1B} + i_{d2B}$
   g. Show that R_o. is equal to ($r_{o1B} \| r_{o2B}$). Magic!
5. A single-stage op-amp has a low frequency gain of 200 and a dominant pole at 10Mrad/sec.
   a. Draw the s-plane with the real axis from -10^7 to 0, and the imaginary axis from 0 to 10^7 . Mark the pole location with an x, and draw a dot at 10^7j.
   b. Draw the vector from the pole to 10^7j. Calculate the magnitude and phase of this vector.
   c. Draw a dot at 10^6j. Draw the vector from the pole to 10^6j. Calculate the magnitude and phase of this vector.
   d. Repeat parts a. and b., but with the imaginary axis from 0 to 10^8 and the dot at 10^8j.
   e. Draw a Bode plot of the gain of your amplifier, with frequency running from 10^5 to 10^9rad/s. Use the straight-line approximations for the Bode plot, and then add dots showing the results of parts b, c, and d.
6. A two-stage CMOS op-amp running at a particular bias point has the following parameters: G_{m1}=1mS, R_{o1}=1MΩ, C_1=0.1pF, Cc=0pF, G_{m2}=1mS, R_{o1}=100kΩ, C_2=10pF.

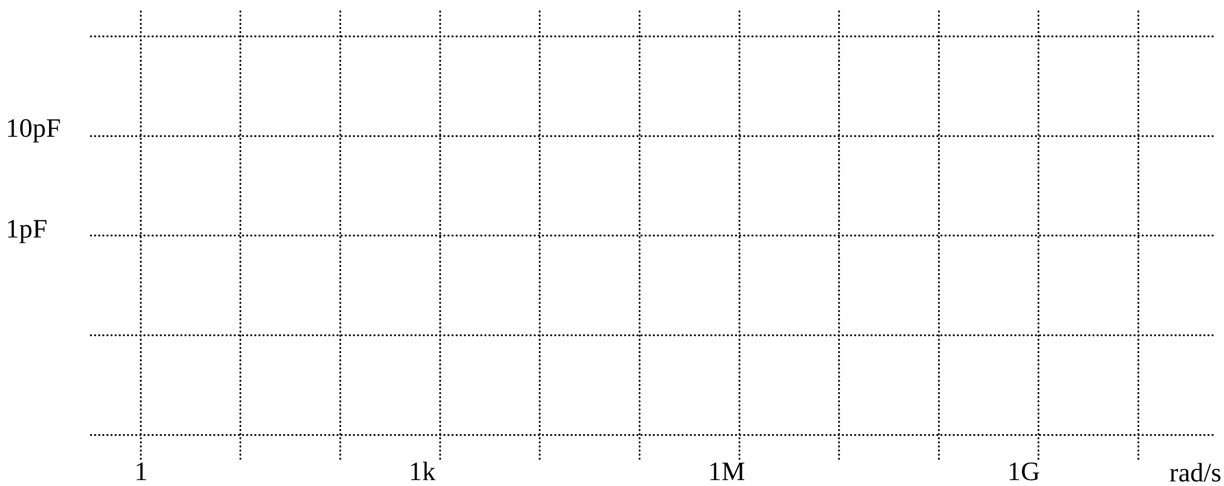
a. Plot the magnitude and phase of the overall gain of this uncompensated amplifier.
b. Where are the poles of the uncompensated amplifier? Is it unity-gain stable?

7. For the same amplifier as above, we now add Cc=1pF. For this problem, you may ignore the RHP zero that this introduces. On the figures provided below,
   a. Plot the magnitude of the second stage gain vs. frequency
   b. Plot the magnitude of the input *capacitance* of the second stage (including C_c) vs. frequency
   c. Plot the magnitude of the input *impedance* of the second stage vs. frequency. Add a line for the output impedance of the first stage.
   d. Now plot the magnitude of the gain of the first stage on the top plot, and the magnitude of the overall gain of the amplifier
   e. What are the compensated poles of the amplifier? If C_c were 0, where would the poles of the amplifier be?
8. [ee240a] For a standard 5 transistor CMOS differential amplifier show that the gain from a differential input to the (so called virtual ground!) tail voltage is 1/4. You can assume that $g_m r_o >> 1$ for all combinations of g_m and r_o. You can win bets with experienced IC designers with this knowledge!

Second stage gain – $|A_{v2,0}|$, and first stage and overall gains



magnitude of second stage input (Miller) capacitance



second stage input impedance, and R_{o1}