EE 140/240A Prof. Pister
Spring 2018

Homework Assignment #2

Due by online submission Monday night 1/29/2018 (Saturday at 9am)

1. Some things you should calculate, some you should just know. I won't let you use calculators on the exams.
    a. Look up the values for Boltzmann's constant and the charge on the electron, and show that k_B/q is about **86 uV/K**. That's a number that you should memorize.
    b. 300 K is a little warm for room temperature (it's over 80 F, which may actually be the room temperature in our classroom). For reasonable values of "room temperature", the thermal voltage V_{TH} is either **25mV or 26mV**. Pick one of those and memorize it. Regardless of the current temperature how much does the thermal voltage change when the temperature goes up by 1 degree Centigrade? How much does the thermal voltage change if the temperature goes from 20C to 70C (upper bound temp requirement for consumer electronics)? Hopefully you didn't use a calculator for those last two.
    c. At "room temperature", calculate V_{TH}*ln(10). Whatever you came up with, remember the phrase "**60 millivolts per decade**". It comes up a lot.
2. You have a diode with N_D=10^18/cm3, N_A=10^15/cm3. You calculate that the depletion width is about a micron.
    a. Is the depletion region mostly in the P side or the N side?
    b. Estimate the built-in potential at room temperature without using a calculator (see problem 1c - if your answer here is not a multiple of 60mV it is wrong.)
    c. If you increase the N doping by a factor of 10
        i. How much does the built in potential change?
        ii. Roughly how much does the depletion width change? (e.g. increase by 10x, decrease by sqrt(10), slight increase, no change, etc.)
    d. If you increase the P doping by a factor of 10, same questions
    e. You apply a reverse bias equal to the built-in potential. Without using a calculator, how much does the depletion region change?
    f. You apply a reverse bias that causes the depletion region to double from the unbiased state. Without using a calculator, what is the junction potential (sum of built-in and the reverse bias)? What is the applied reverse bias?
3. You have an array of identical diodes on a silicon chip. They all have a forward voltage of 0.6V with a current of 10uA.
    a. if you pass 10uA through a series connected array of 10 diodes, what voltage do you measure?
    b. if you pass 10uA through a parallel connected array of 10 diodes, what voltage do you measure?
    c. if you apply 0.6V to a series connection of 2 diodes, what current do you measure?
    d. if you apply 0.6V to a parallel connection of 2 diodes, what current do you measure?
    e. if you apply -0.6V to a single diode, roughly what current do you measure? (the answer is not 0 - estimate I_S)
4. In an NPN transistor in forward active,
    a. collector current increases with increasing V_{be} bias because: (your answer should say something about either n or p type carriers, and drift and diffusion currents)
    b. collector current increases with increasing V_{CE} because: (your answer should say something about what is happening in the base, and how that relates to either n or p type carriers, and either diffusion or drift)
5. In an NMOS transistor in saturation,
    a. drain current increases with increasing Vgs because: (your answer should say something about n or p type carriers, and why there is more or less of them)

b. drain current increases with increasing Vds because: (your answer should say something about what is happening in the channel, and how that relates to either n or p type carriers, and either diffusion or drift)

6. In a PMOS device, the charge on the gate is balanced by what types of charges (electrons, holes, positive or negative ions) in these regions of bias:
   a. in accumulation
   b. in sub-threshold
   c. in inversion
7. For a 1um NMOS transistor with V_{tn}=1V in a circuit with V_{dd}=3V, sketch the regions of operation in a figure with Vds on the horizontal axis and Vgs on the vertical axis. Label where the device is OFF, TRIODE, SAT, and SUB-Vt. Draw a dotted line and label the quadratic and velocity saturated regions.
8. Real devices do not always fit our simple models very well. The PMD3001 has an NPN and PNP bipolar transistor in the same package. Use the datasheet to answer these questions. https://assets.nexperia.com/documents/data-sheet/PMD3001D.pdf
   a. Looking at figure 6, estimate the NPN output resistance r_o and Early voltage V_A when
      i. I_C=0.8A and I_B=3.4mA
      ii. I_B=1.7mA and V_{CE}>2V
   b. Looking at figure 7, near room temperature there is a fairly straight line relating V_{BE} to I_C over three decades of collector current from 0.1mA to 100mA.
      i. What does our theoretical model say the slope of that line should be?
      ii. What is it in the figure?
   c. Also in figure 7,
      i. the slopes are different at different temperatures. Why? Are they consistent with our model?
      ii. for a fixed collector current, the base-emitter voltage decreases with temperature. Why?
      iii. At V_{BE}=0.7V, how much does the collector current change from -55C to 25C? What does that say about the change in I_S?
9. The 2N7002P is a discrete NMOS transistor that costs $0.017 in volume on digikey.com. https://assets.nexperia.com/documents/data-sheet/2N7002P.pdf .
   a. From figure 6, estimate the threshold voltage, and the transconductance when V_{GS}=2.5V. Can you estimate the output resistance when V_{DS}=V_{GS}=3V? Why or why not?
   b. From figure 7, estimate the typical sub-threshold slope, and the value of the parameter n.
10. Look at the 2014 paper on the Intel 14 nm FINFET.

a. From Figure 5, estimate g_m, r_o, and intrinsic gain for NMOS and PMOS transistors when V_{GS}=0.5V and V_{DS}=0.5V (PMOS values are negative). Note: the vertical axis in Figure 5 is mislabeled! It should be mA/um, not A/um. Figure 6 is correct.

b. From Figure 5, estimate roughly what V_{TH} is for NMOS and PMOS devices. Do these devices look exponential, quadratic, or velocity saturated? Why?

c. From Figure 6, estimate the subthreshold slope and the parameter "n" for NMOS and PMOS devices.

11. For an NMOS transistor with W/L=10u/1u, with $\mu_n C_{ox}$=100μA/V^2, V_{DD}=3V, λ=1/(10V), and V_{TH}=1V.

a. Carefully sketch by hand the drain current vs. V_{DS}=0 to 3V at constant V_{GS}=0, 1, 2, 3V.

12. Do the same for a PMOS transistor of the same size with the same parameters except V_{DS}=0 to -3V and V_t=-1V. You should get exactly the same plot, just rotated 180 degrees and with different axis labels.

13. [240a] Find at least two recent research papers on interesting transistors and calculate intrinsic gain. e.g. nanotubes, graphene, WS2, 7nm, organic, ...