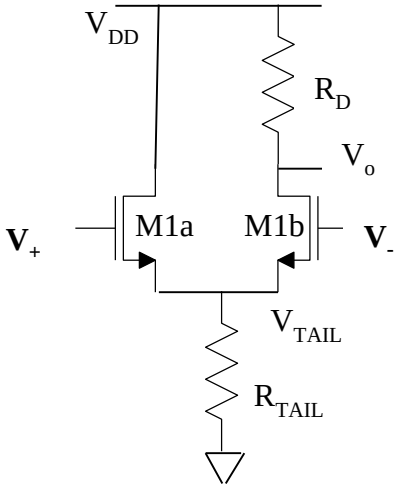
EE 140/240A Prof. Pister
Spring 2018

Homework Assignment #5

Due by online submission **Wednesday** 3/4/2018 (Thursday 9am)

1. We usually approximate the closed loop gain $A_0/(1+A_0f)$ by 1/f. How good or bad an estimate is that? Show that the fractional gain error (gain_error/gain) is $-1/(A_0f)$.
2. In a single pole op-amp with A_0=100,000 , ω_p=1k rad/s, a feedback factor of f=0.01 is used. Find:
   a. the exact low-frequency closed loop gain $A_0/(1+A_0f)$ (use a calculator if needed)
   b. the approximate low-frequency closed-loop gain, 1/f
   c. the fractional gain error, using the result from the previous problem. Does it agree with your results above?
   d. Above the pole frequency, amplifier gain decreases, and gain error increases. What is the fractional gain error at $10\omega_p$? $100\omega_p$?
3. Check out the datasheet for the LM324 quad op-amp. http://www.ti.com/lit/ds/symlink/lm324.pdf There's a schematic on page 2. Redraw (or cut and paste) that schematic, and identify (circle and label)
   a. input differential pair (Darlington)
   b. current mirror active load
   c. emitter-follower level shifter(s)
   d. compensation capacitor
   e. common emitter amplifier (Darlington)
   f. output stage
4. Assuming the same process parameters (e.g. V_A, β), how will the performance of the LM324 design compare to the amplifier that you built in Lab3 in the following areas
   a. Input impedance. How does bias current and Darlington affect this?
   b. Impedance at the output of the first stage? How does the emitter-follower affect this?
   c. Output impedance of the amplifier. How does output stage affect this?
5. Given a diode-connected NPN transistor Q1 which has a 6uA reference current flowing through it, design a bipolar circuit to generate all four of the current supplies shown in the LM324 schematic. The 50uA and 100uA currents don't need to be exactly right, but should be close. Label your transistors as multiples of each other as appropriate, e.g. Q2=5Q1. You may assume infinite beta.
6. For the differential amplifier in the figure below you may assume that the transistors have λ=0. Estimate the change in Vtail, Itail, Id1a, Id1b, and Vo due to
   a. An increase of ΔV in both V+ and V-
   b. An increase of $\Delta V/2$ in V+, and $-\Delta V/2$ in V-
   c. An increase of ΔV in just V+
   d. What is the common mode rejection ratio of this amplifier?
   e. What is the common mode input range in terms of V_{tn} and V_{ov}?
   f. Sketch V_{ov} vs. V_{cm} over that input range.
   g. Sketch the bounds of the output swing over that input range.



7. Now answer questions a, e, f, and g above for an NMOS-input 5 transistor CMOS differential amplifier, with non-zero λ.
8. Design a 2-stage NMOS input CMOS op-amp with the following specs:
   a. 80uA tail current
   b. able to sink 200uA from the load
   c. output swing to within 200mV of the rails
   d. input common mode range to within 200mV of the top rail

   Process specs $\mu_n C_{ox}$=200μA/V^2, $\mu_p C_{ox}$=100μA/V^2, λ=1/(5V), $-V_{tp}=V_{tn}$=0.5V, V_{DD}=2V, L_{min}=0.5um, C_{ox}=5fF/um^2, C'$_{ol}$=0.5fF/um. You may use 1 resistor in your design.
   Draw the schematic, and label the device sizes.

9. For the amplifier in the previous problem,
   a. calculate and tabulate Id, V_{ov}, g_m, r_o, C_{gs}, and C_{gd} for all devices
   b. calculate the 1st and 2nd stage gain, and the overall gain for both differential and common mode signals.
   c. calculate the common mode input range, and the variation in tail current over that range.
   d. calculate the gain across Cgd1a.
   e. calculate the output pole frequency with a 100fF load capacitance.
   f. calculate the input capacitance of the second stage for frequencies below the output pole frequency
   g. calculate the first stage output pole frequency, assuming that it is lower than the output pole
   h. calculate the input capacitance of the second stage above the second stage unity gain frequency

10. [ee240A] For the current supplies that you designed for the LM324 above, estimate the actual current assuming a transistor beta of 100. Use a beta helper (Figure 4.6 GHLM, or google "beta helper current mirror") to alleviate this problem. How much did the accuracy improve?
11. [ee240A] If the same amplifier were run at Vov=0, how will that affect the gains and pole frequency?